

# A78DD-M2T (RS780D+SB750) A78GD-M2T (RS780 +SB710) A76GB-M2T (RS780L+SB710)

## REV 6.1

AMD      AM2+

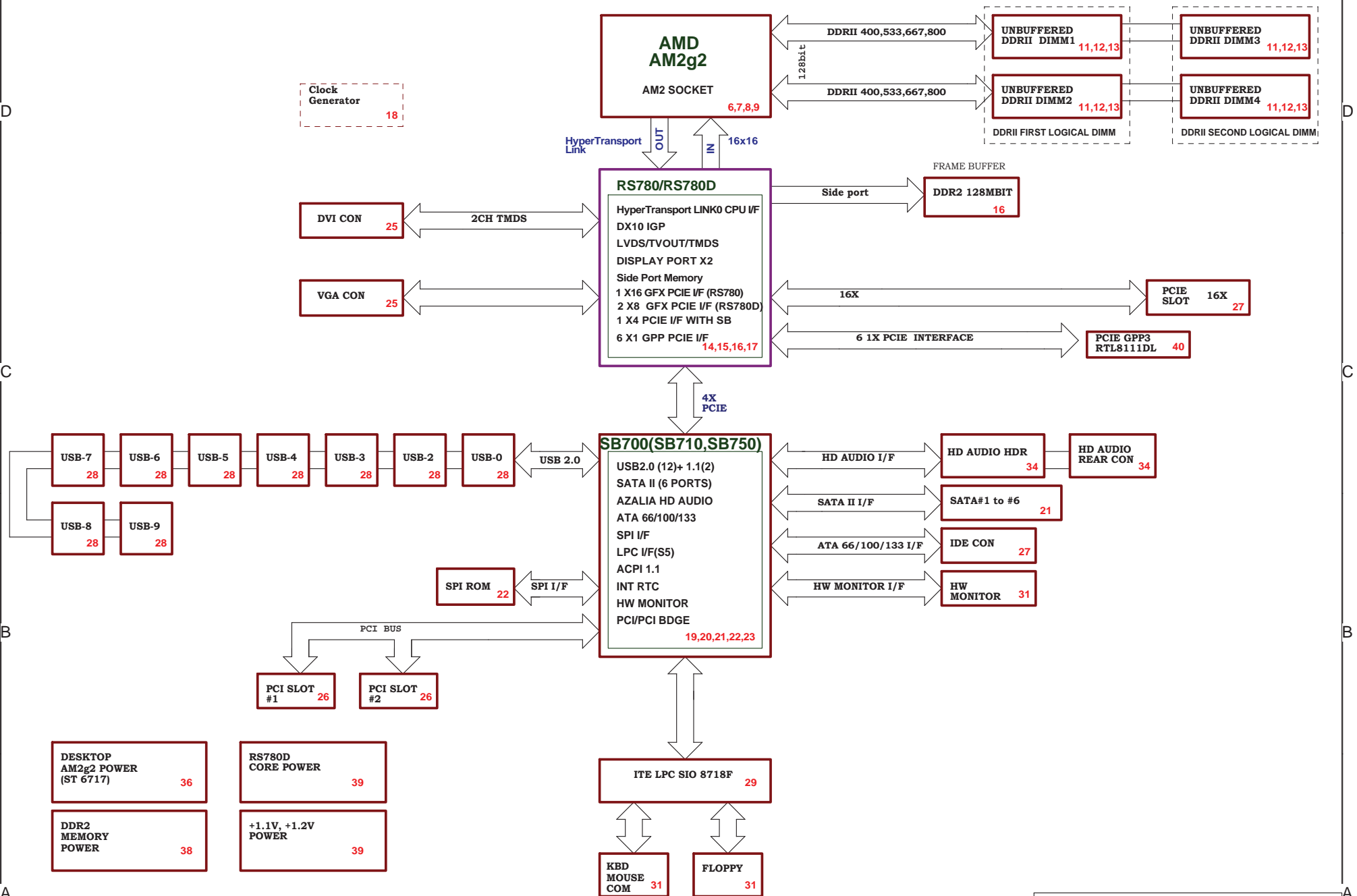
DDR2      X 4      (Dual channel)

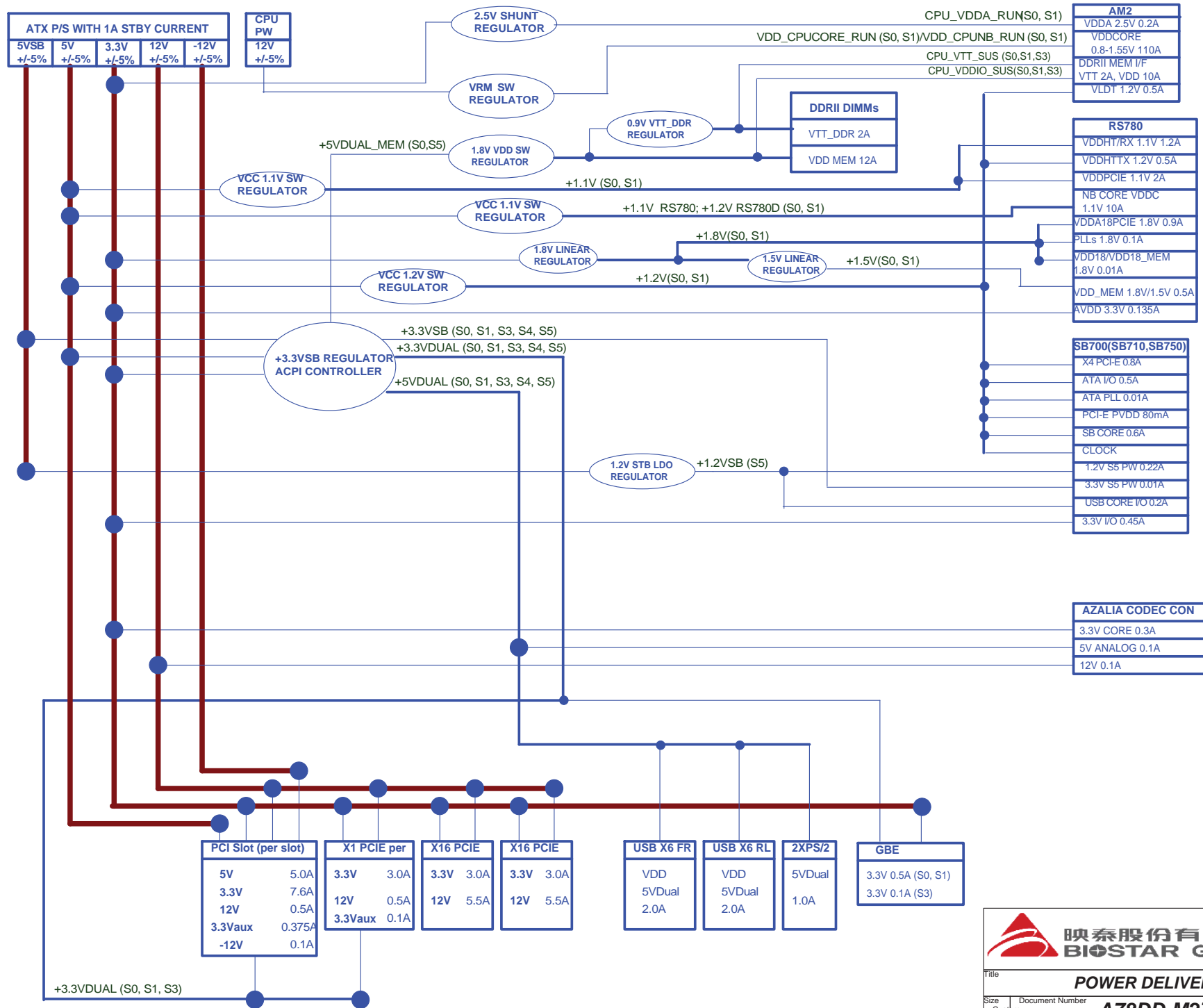
PCI-Ex16 X 1

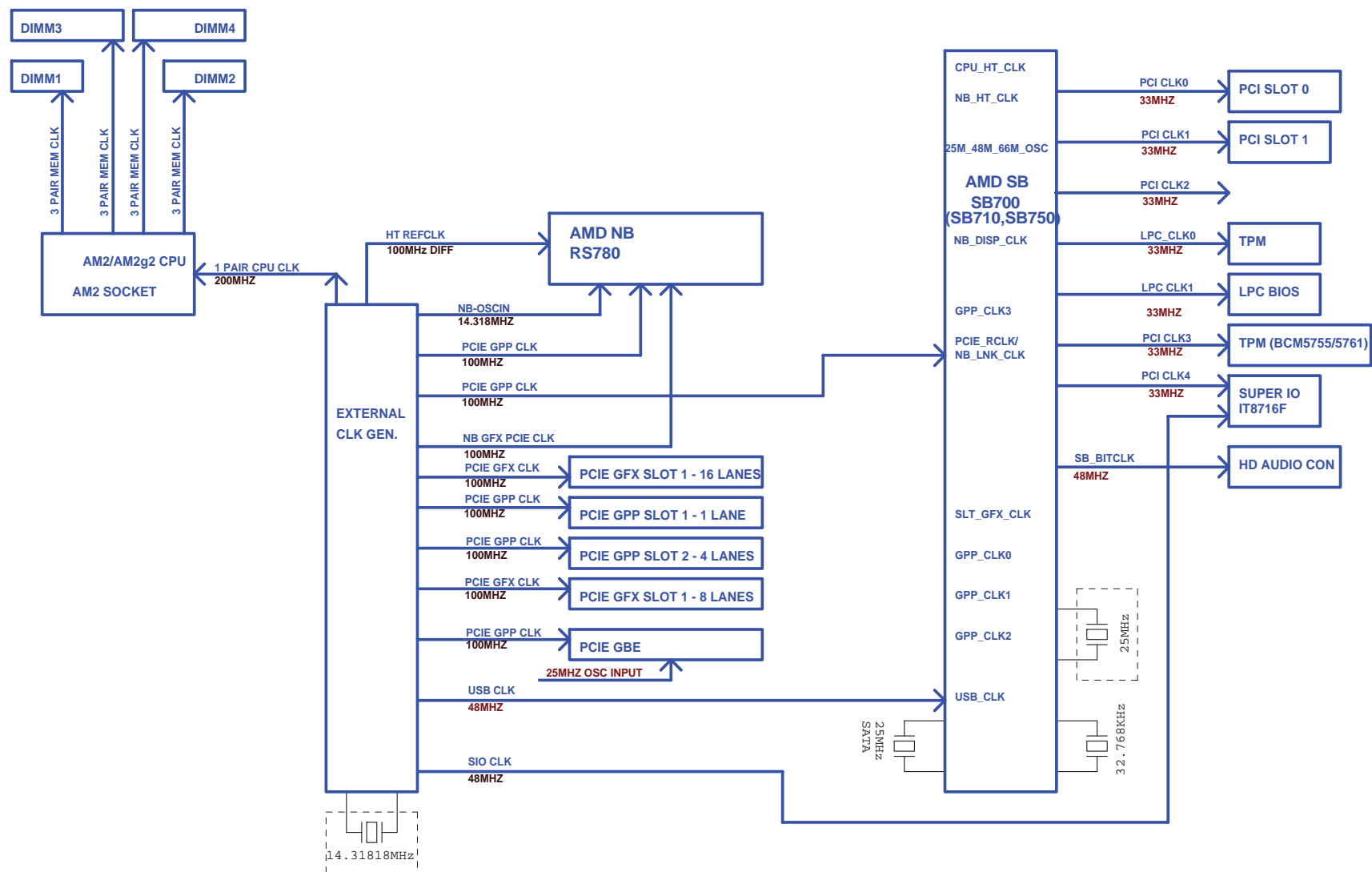
PCI      X 2

RELTEK 10/100/1000 PCI-E Lan

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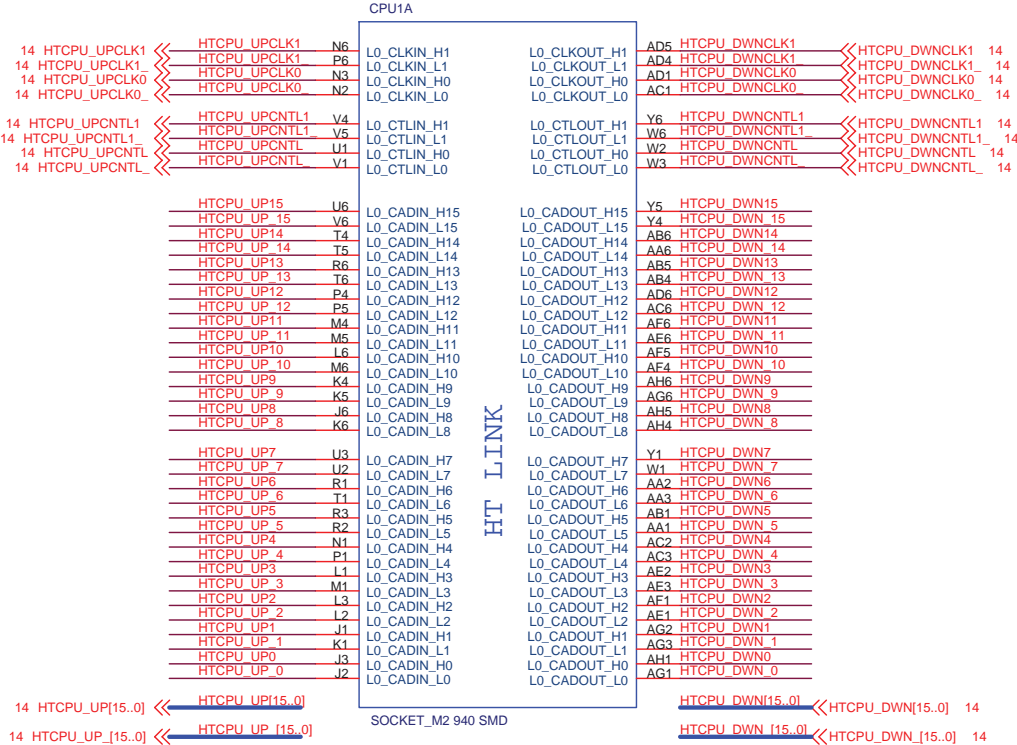
REV	DATA	DESCRIPTION
0.6	02/02/09	1.由A78DF-M2T V0.5修改(新案子)
6.0	03/18/09	1.修改S3問題 (P37) Add R225,Q36  2.移除ACCT功能 (P7,P35) 3.修改VDDHTTX電源(+1.2V-->+1.1V) (P17) 4.Remove R83 C292 (P20) 5.修改VQ1電源(+3.3V-->+5V) 6.修改DVI1 GND(IO_GND-->GND) 7.移除SIO ATX_PWRGD線路 8.修改MH4 GND(GND_AUD-->GND) 9.修改SR39 SR40(10K-->51) 10.Remove AR47 AR48 11.移除GPIO超壓線路(VCPU_NB) (P35) 12.修改 PR60 PR61 PR62 PR63 (1K-->1.1K) (P36) 修改 PR122 (1.5K-->4.75K) 修改PC68 GND (SGND-->GND_PAD) 13.移除 R359 Q62 Q64 Q63 線路 (P37) 修改R220電源(+5V-->+5V_DUAL) 修改PR118 (39k-->1K) 修改PR119 PR120 (10K-->1K) Add PR131 PR130 (330) 修改PR102 (3.01K-->330) 修改R361 (1K-->442) 修改R366 (511-->649)  14.修改CT9(270UF-->560UF 固態) (P38) 修改R235 (2K-->360) 修改R238 (4.37K-->249) 修改Q39電源(+5V_DUAL-->+5V_STBY)  15.修改 CT19 (1000UF-->560UF固態) (P39) 修改R253 (2K-->113) 修改R254 (3.83K-->200)

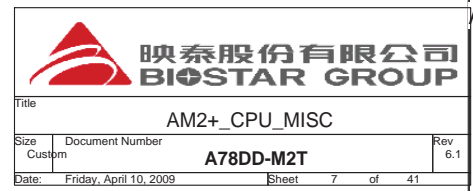
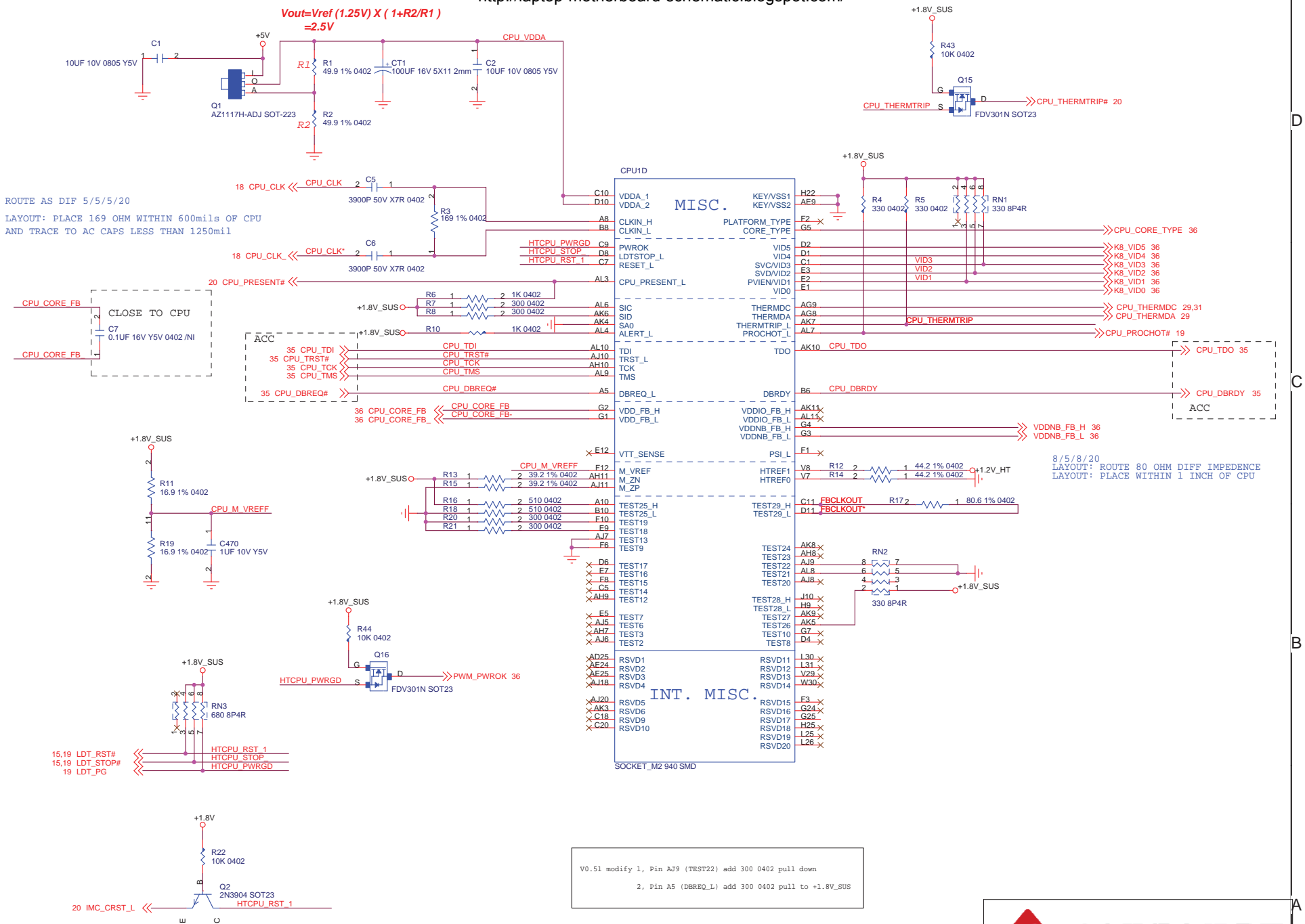


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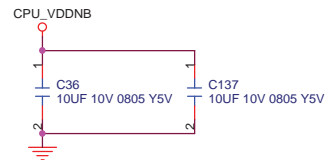
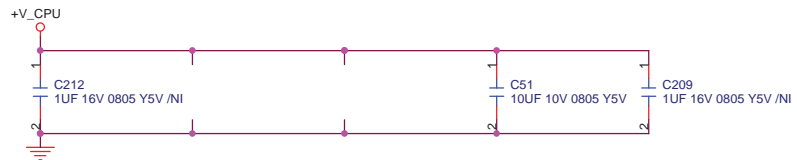
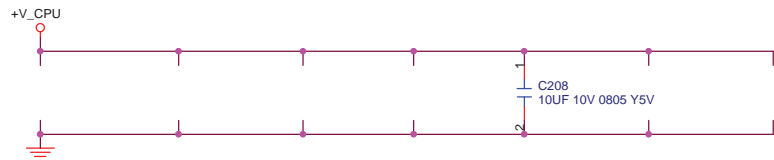
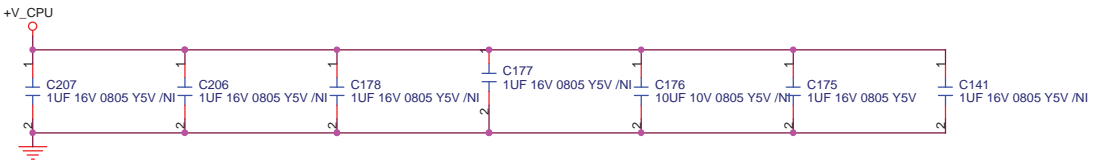
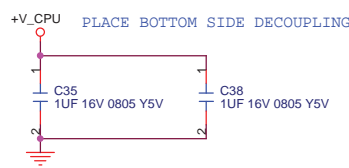
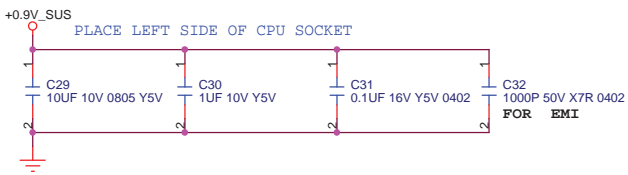
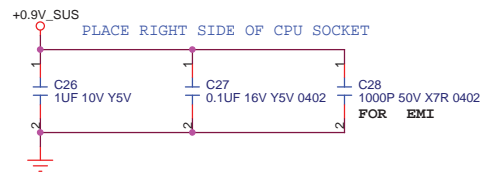
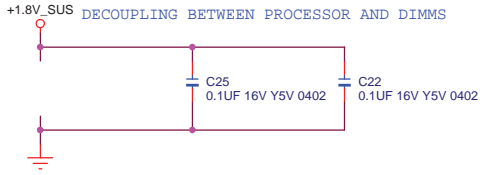
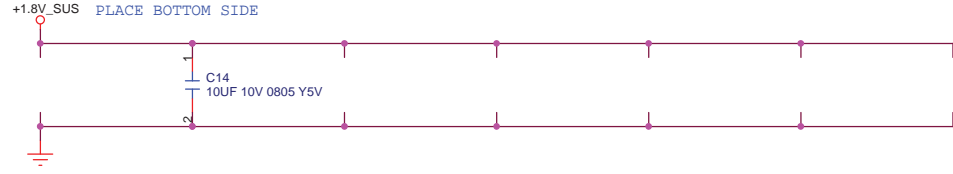
HyperTransport










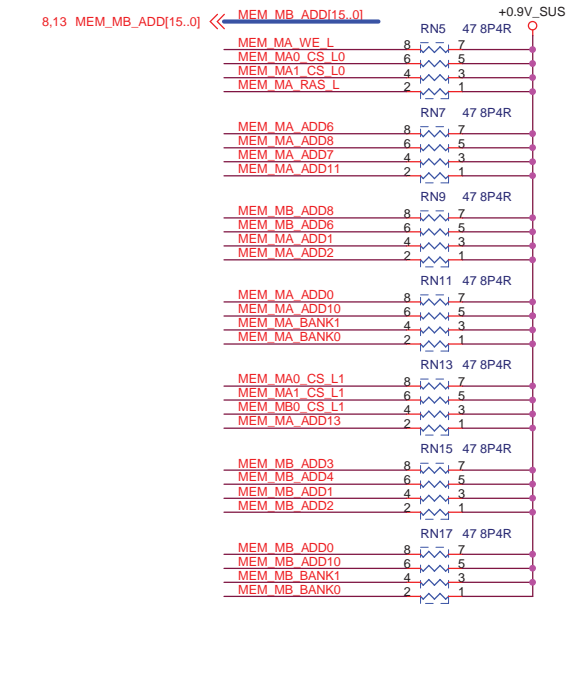
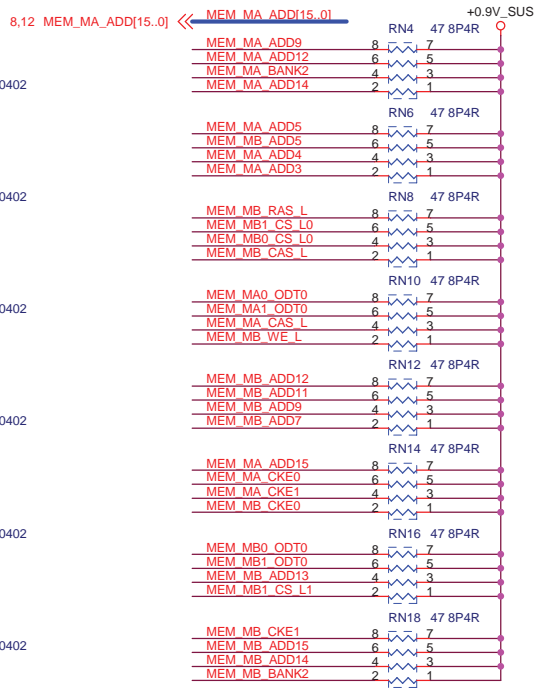
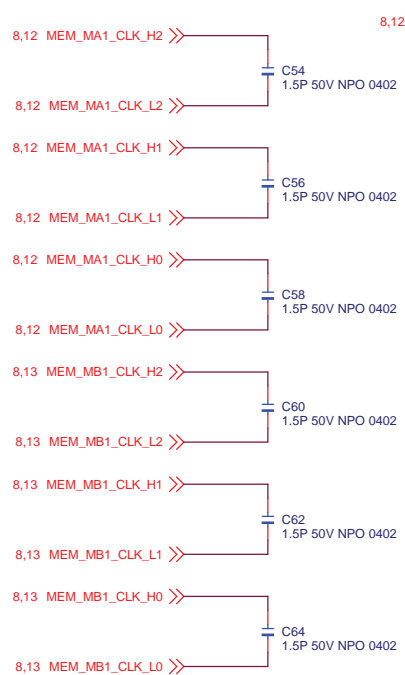
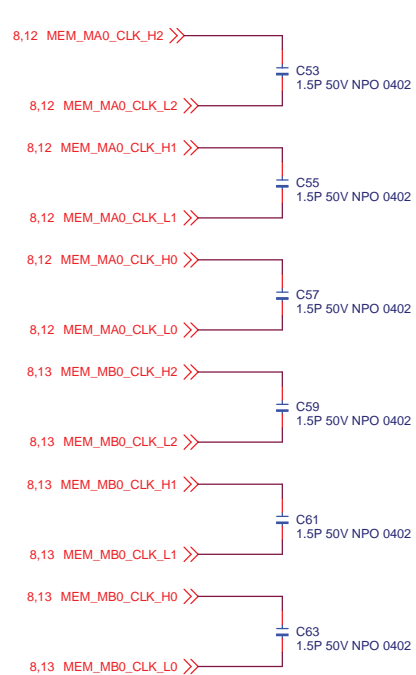




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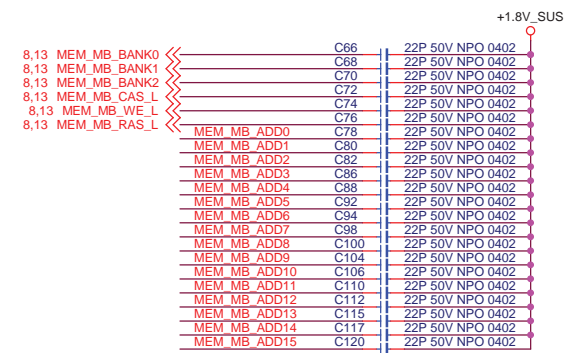
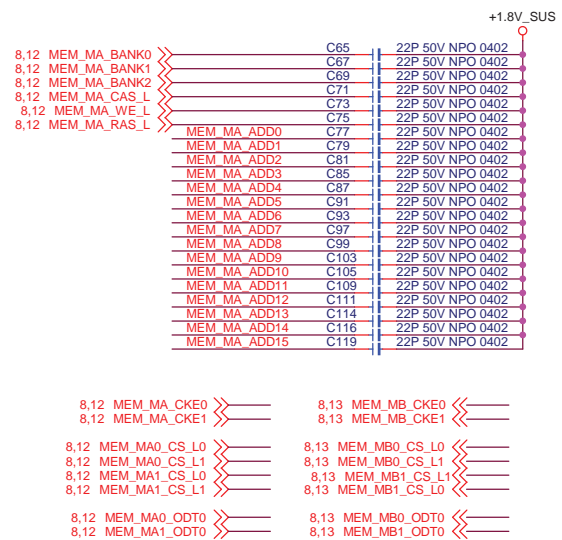
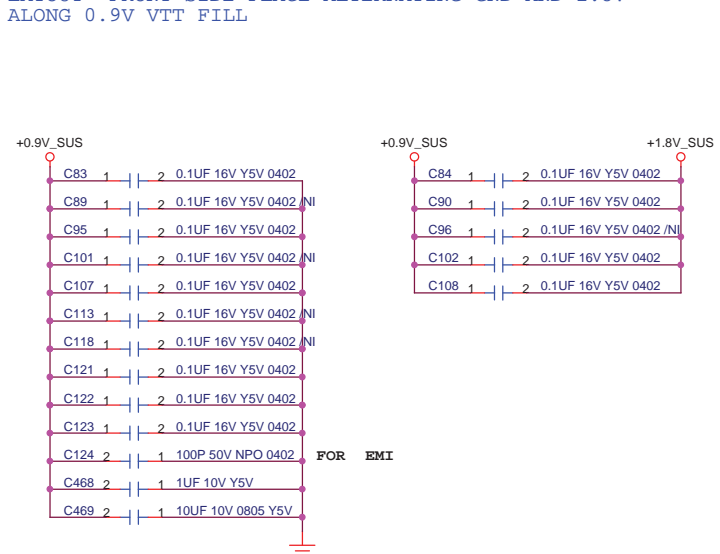
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D



LAYOUT: FRONT SIDE PLACE ALTERNATING GND AND 1.8V  
ALONG 0.9V VTT FILL

B



Title: VTT TERMINATI

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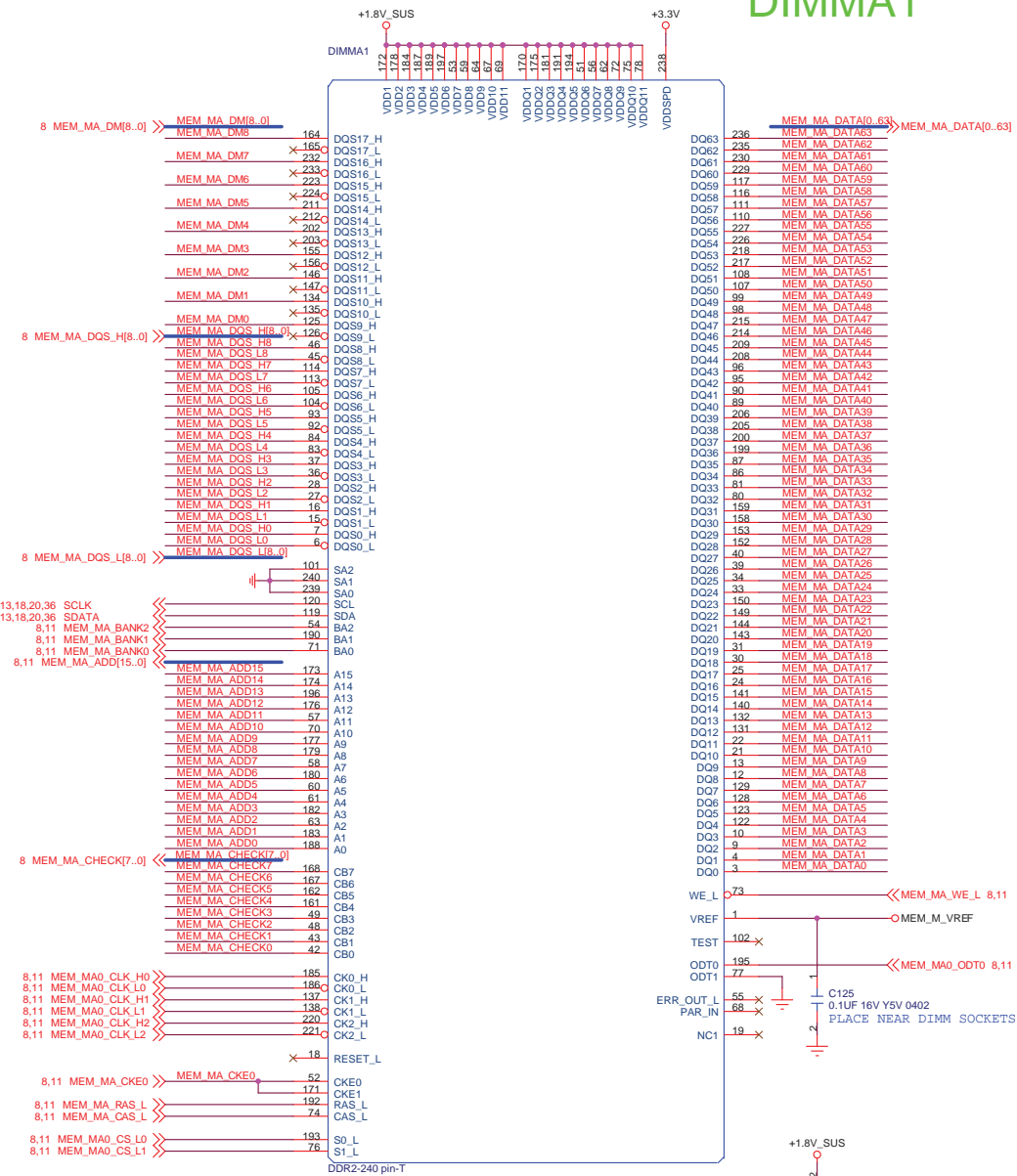
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C

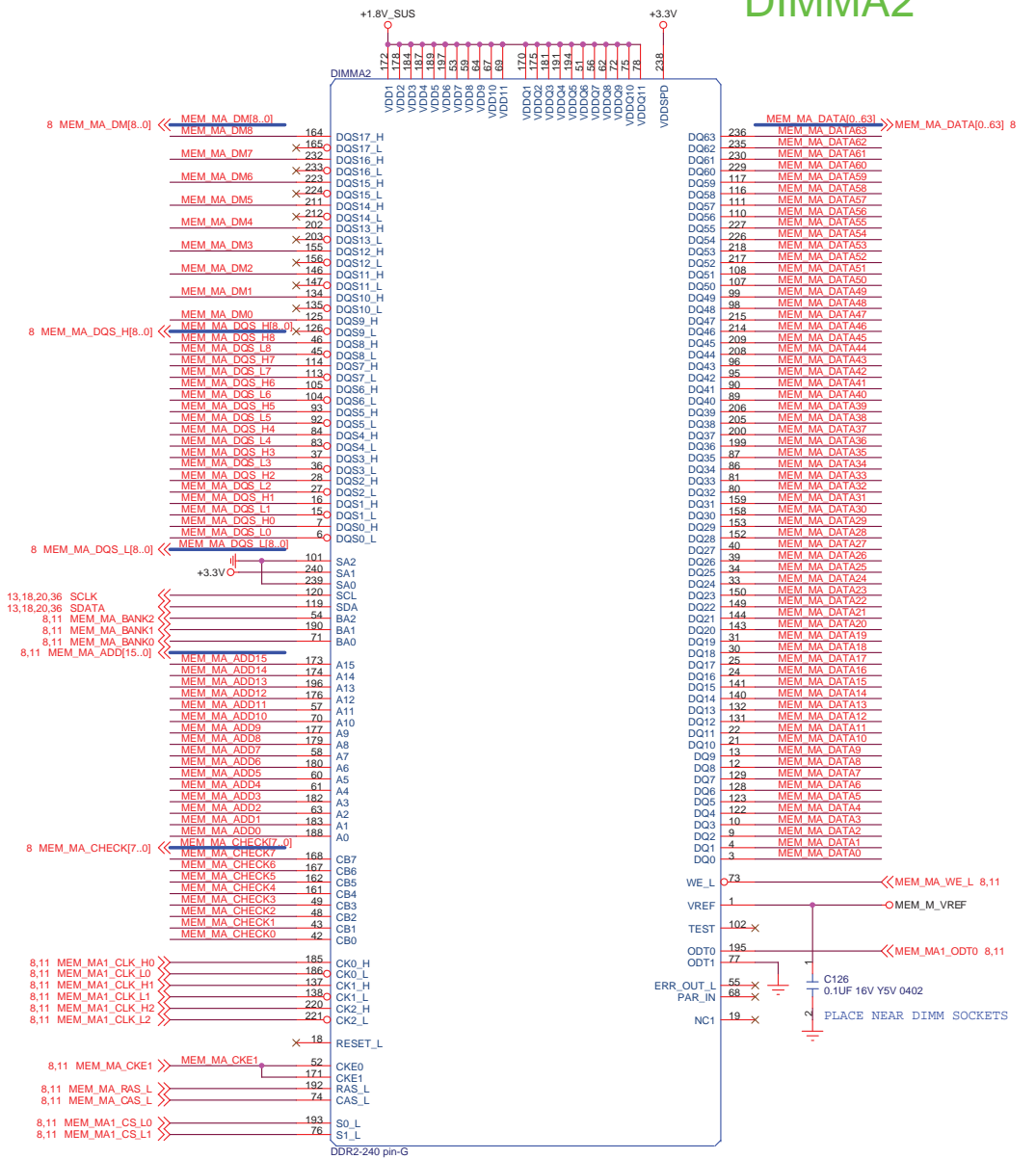
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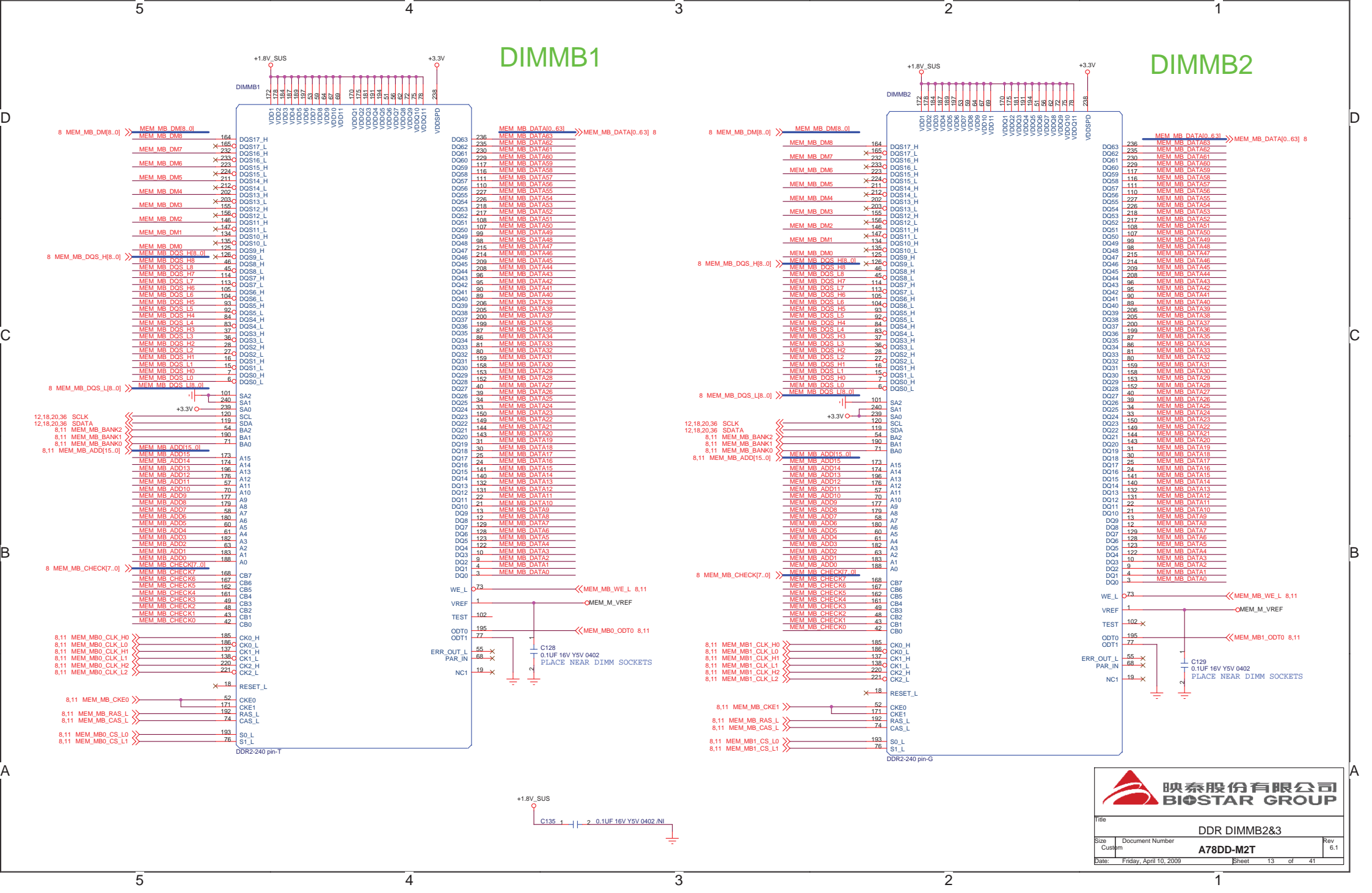
A

## DIMMA1

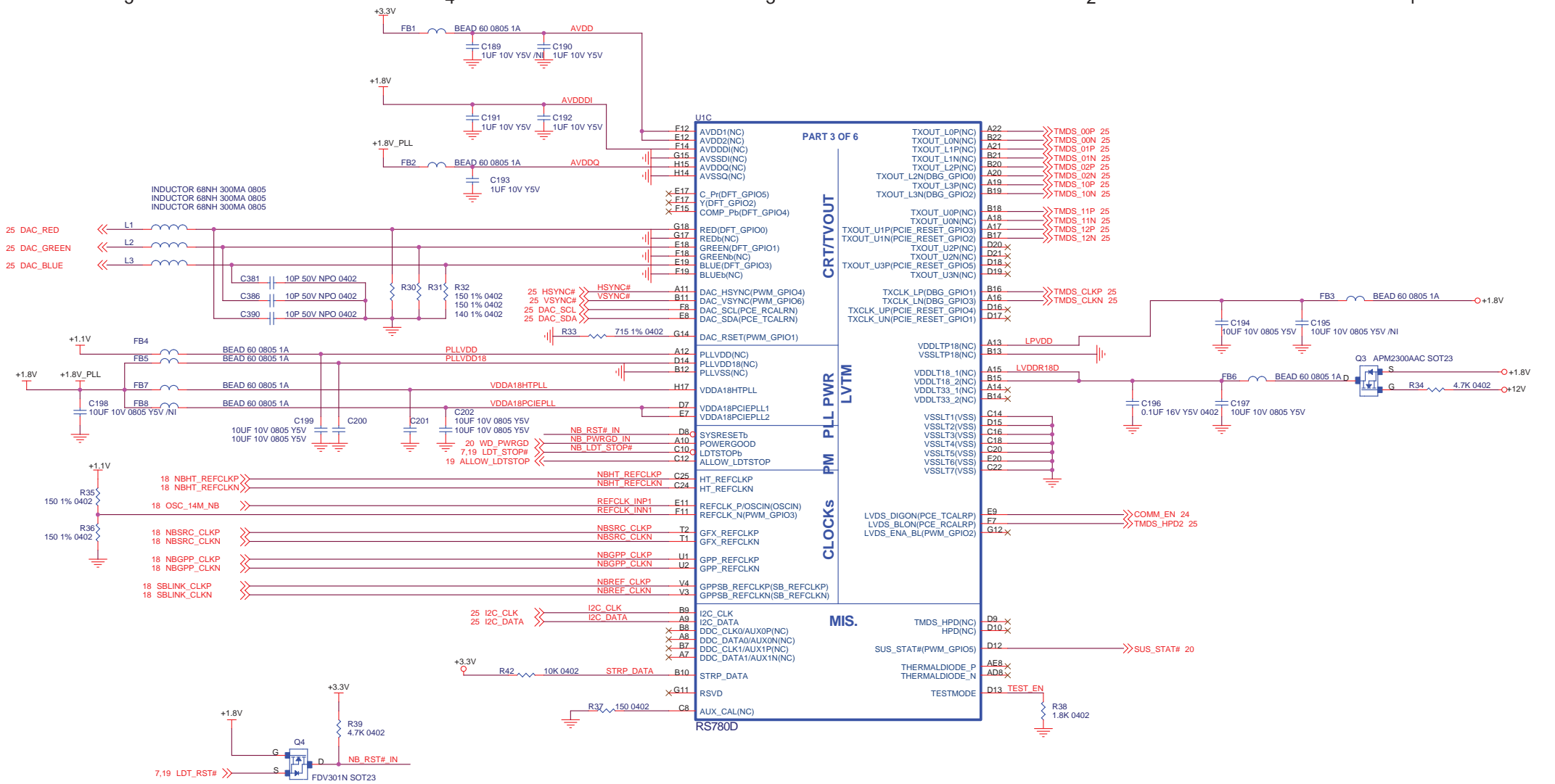


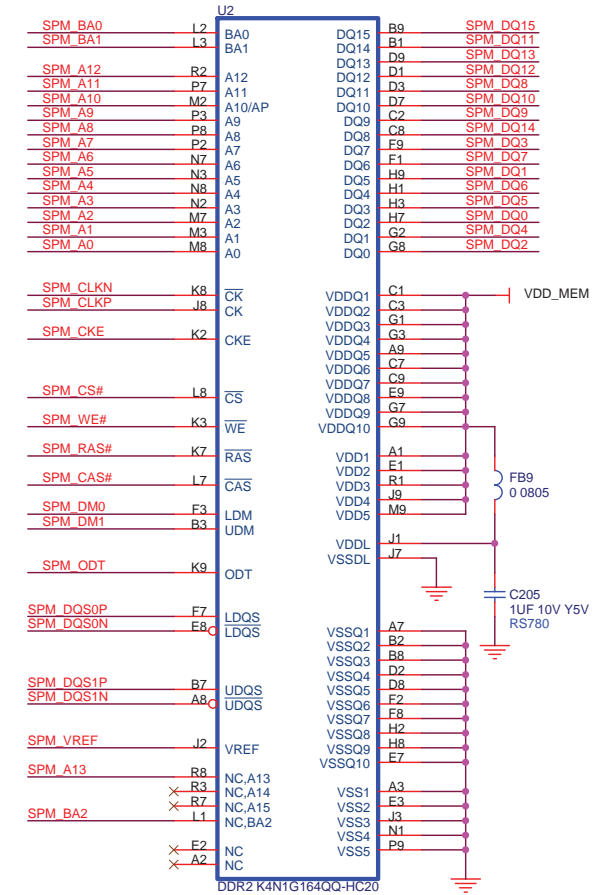
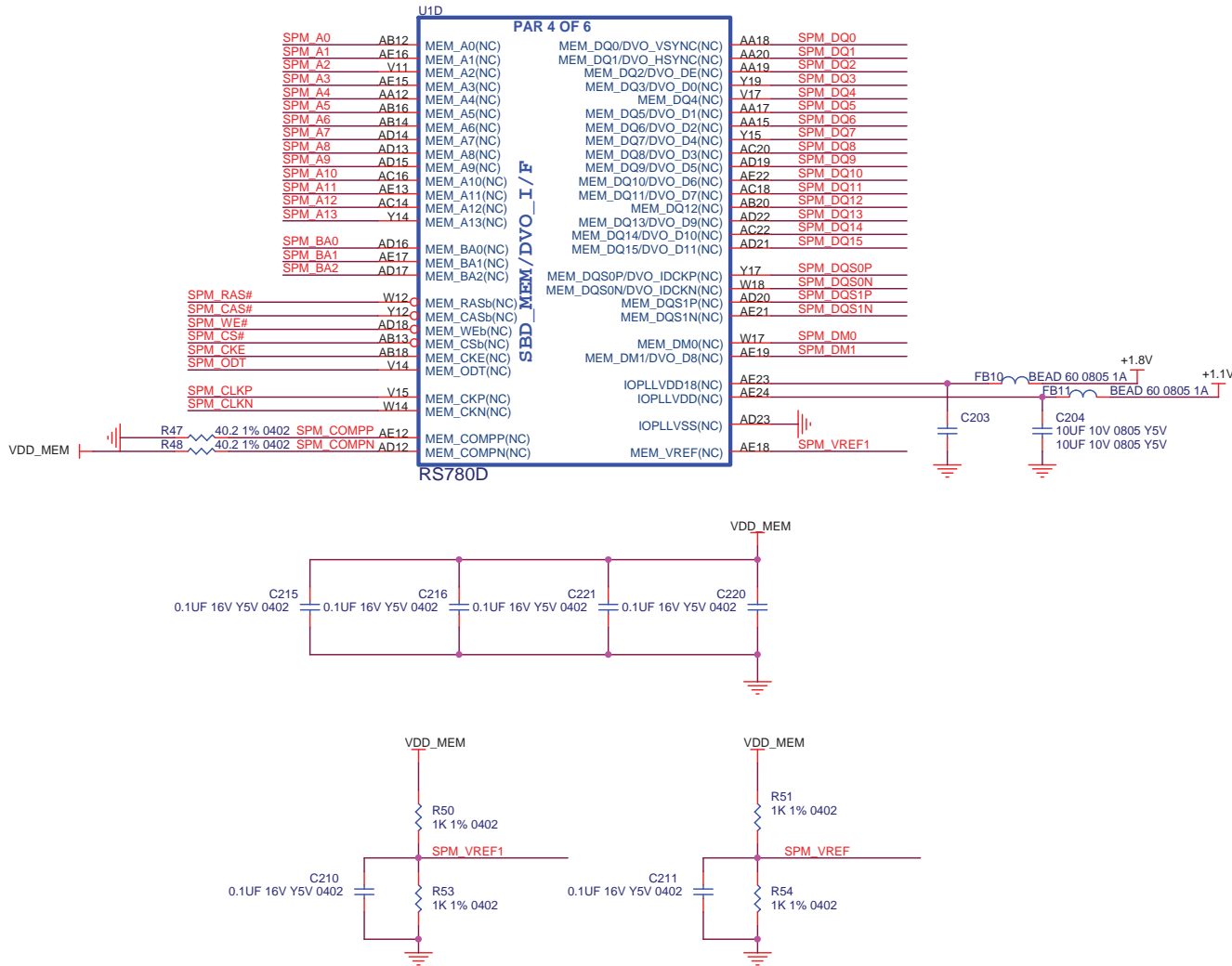
## DIMMA2














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Title

**RS780D SPMEM**

Size B

Document Number

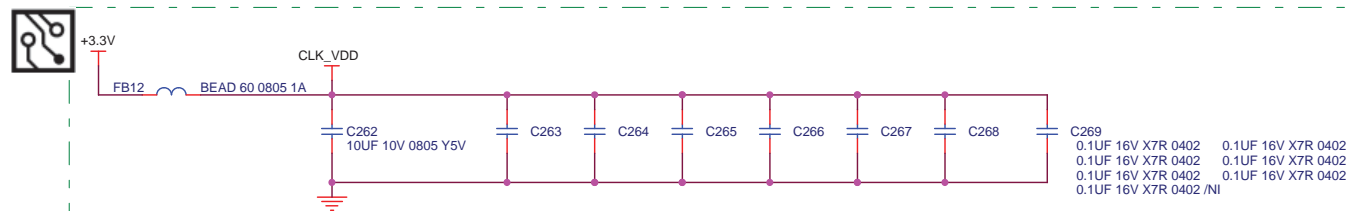
**A78DD-M2T**

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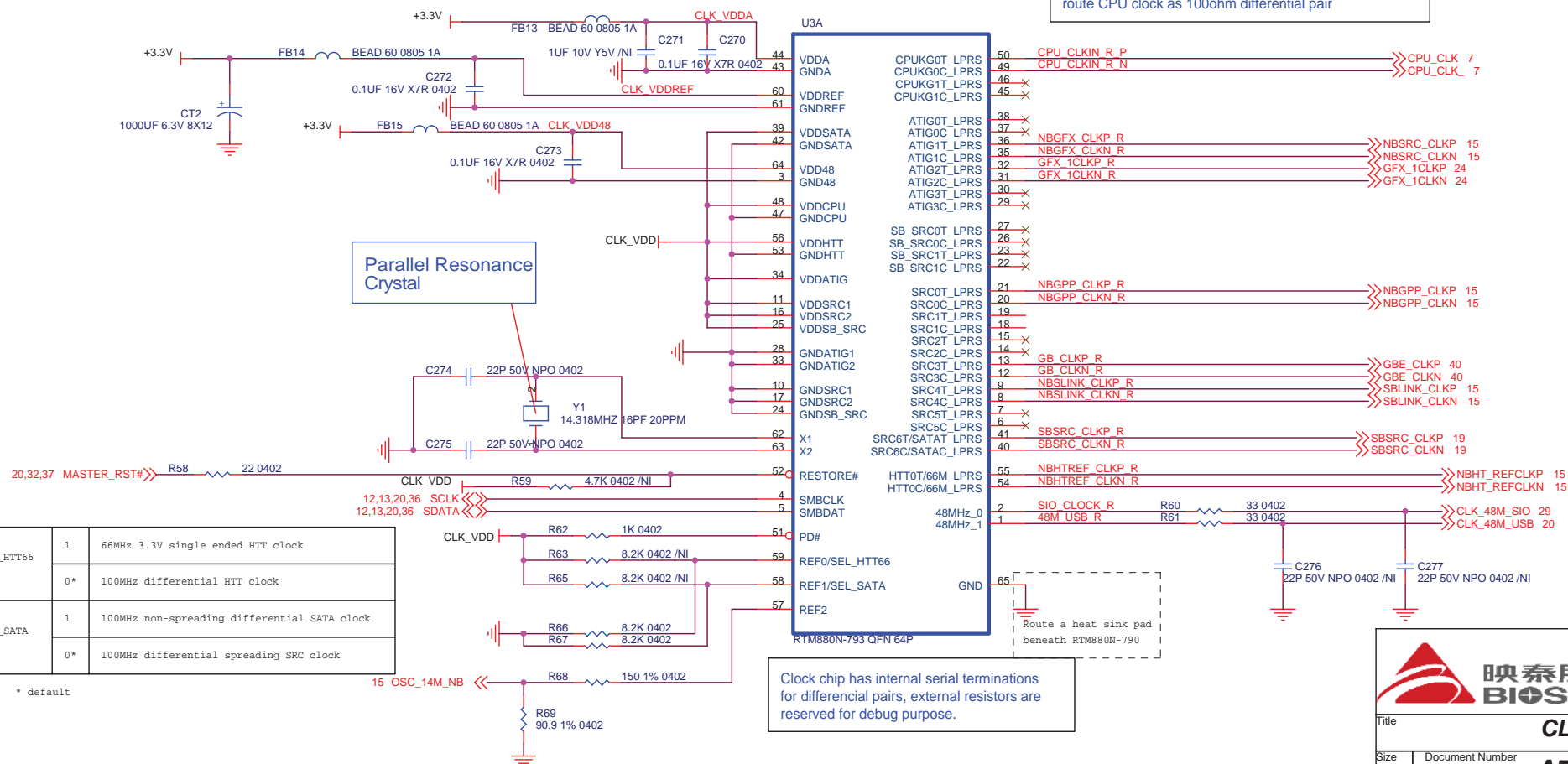
```

1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE TO U800 AS
2-050804 2-050804 ALL SRCCLKTx AND SRCCLKCx
3- AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800
POWER PIN

```



Place R800/801 less than 500 mils away from U800  
R851 less than 100 mils away from R800/801  
route CPU clock as 100ohm differential pair



SEL_HTT66	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock
SEL_SATA	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock

\* default

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

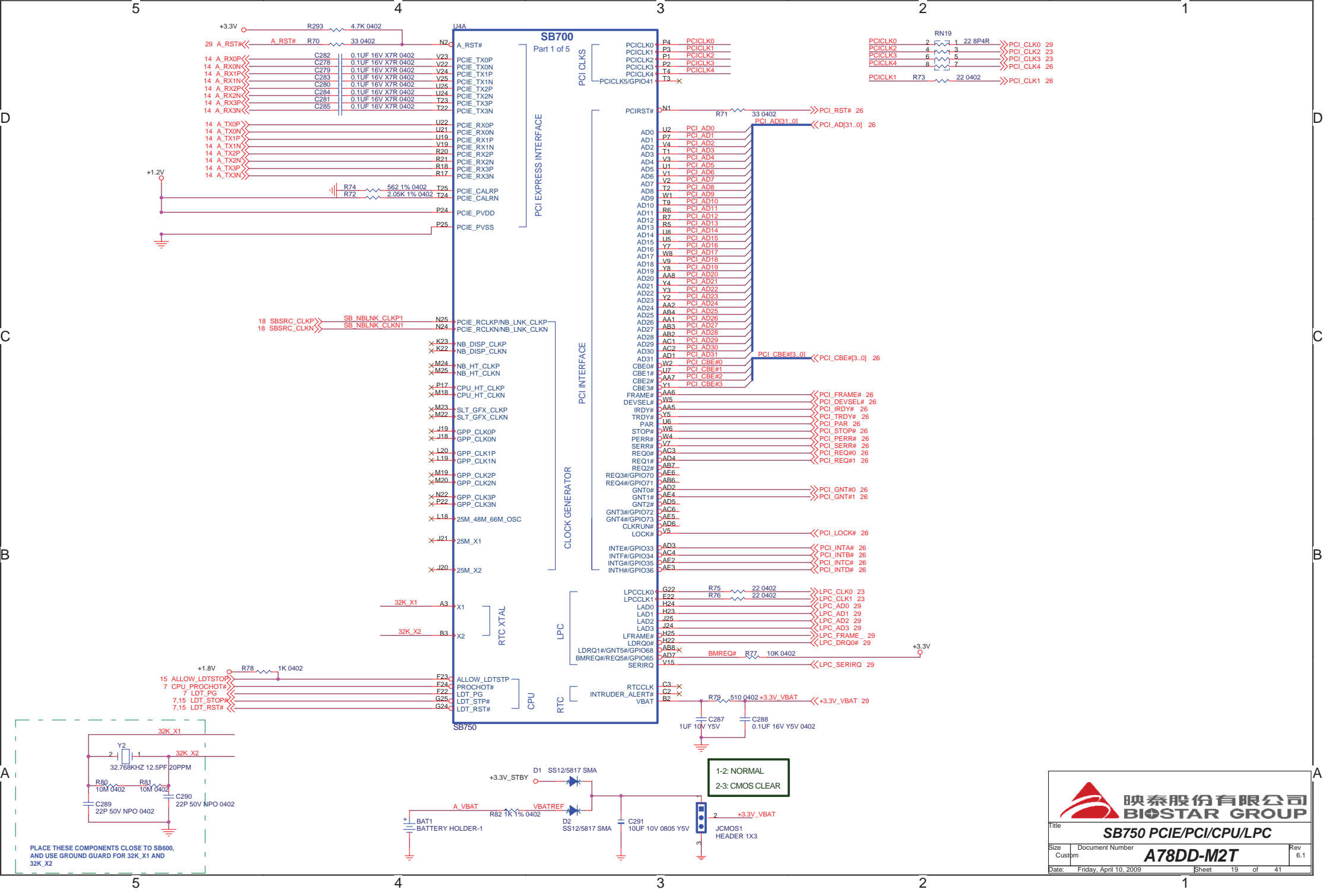


Title	<b>CLOCK GEN</b>
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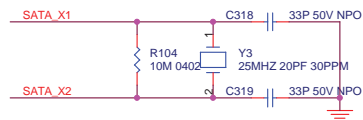
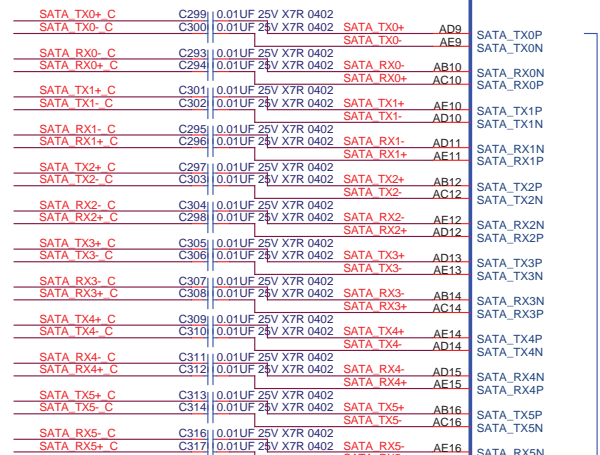
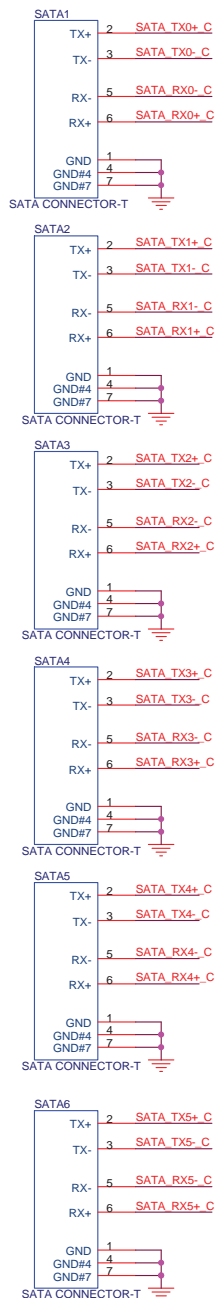
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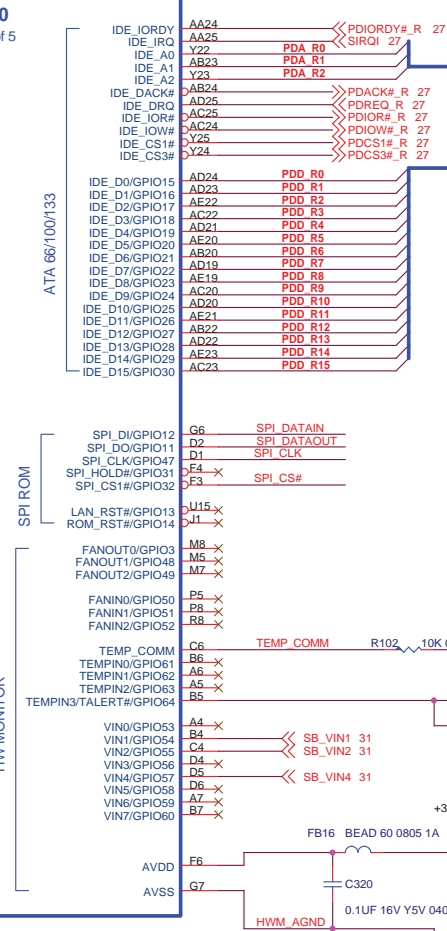


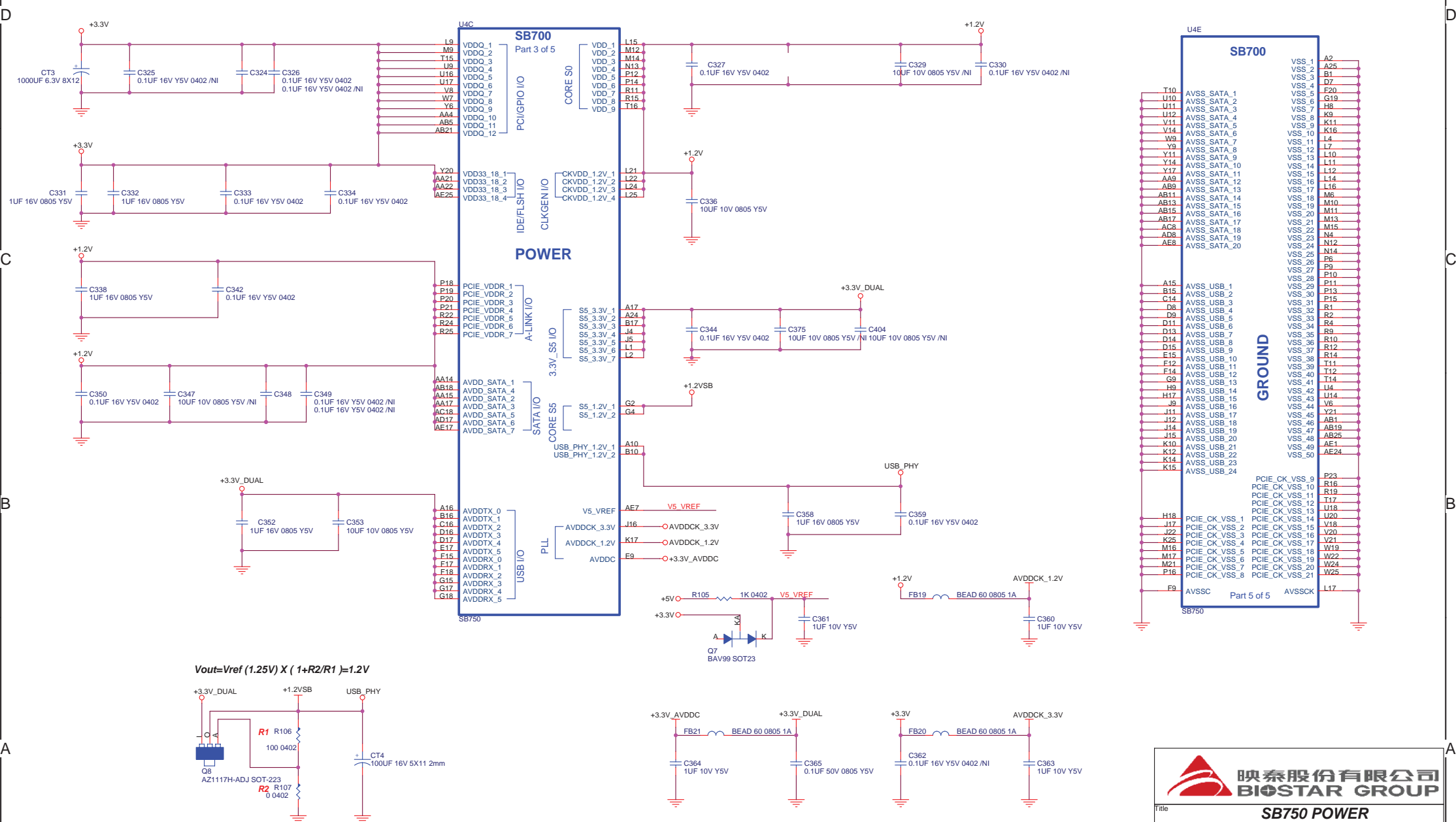


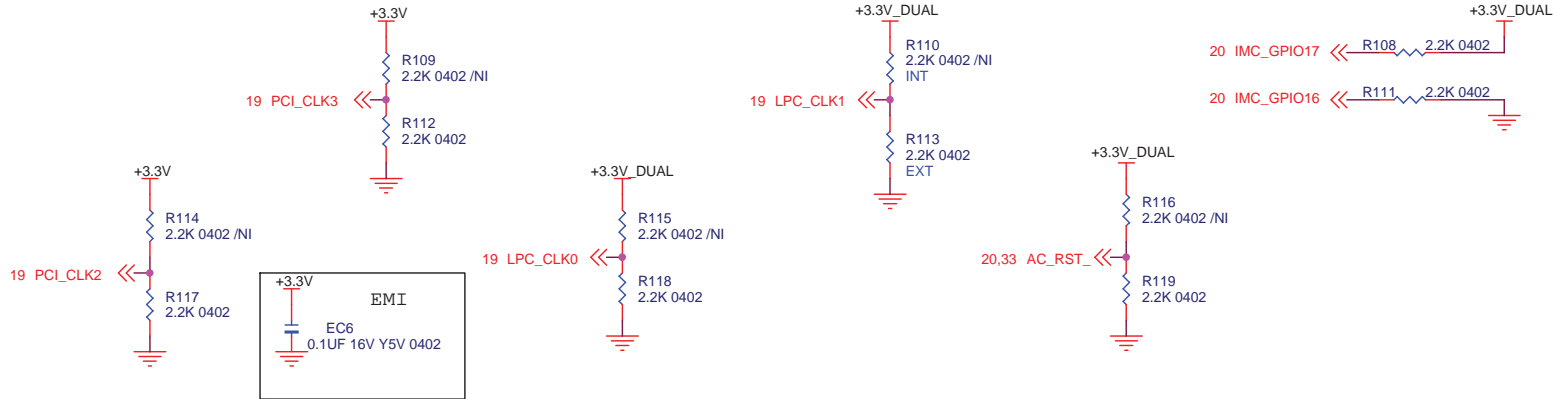
SERIAL ATA

SATA PWR

HW MONITOR



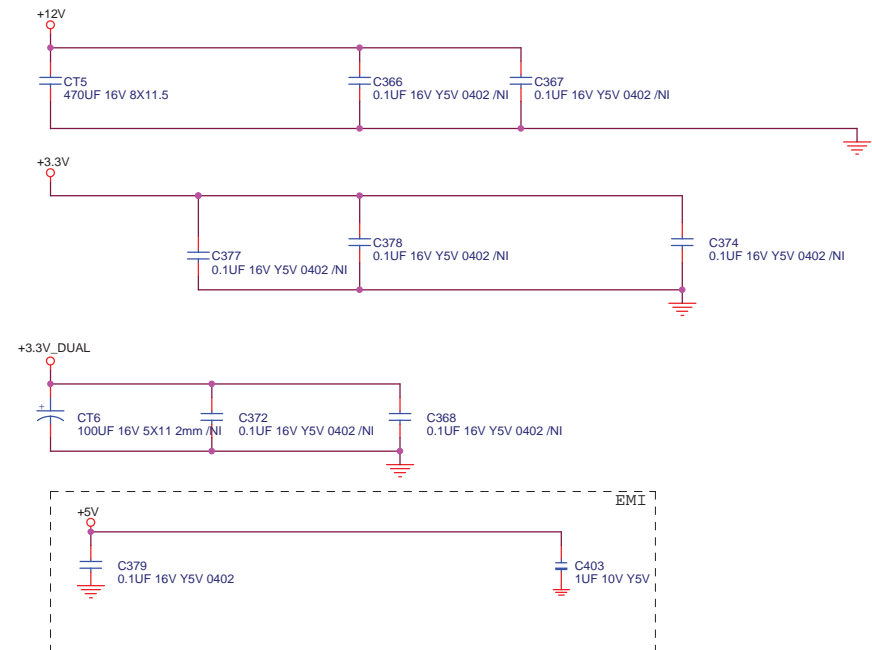
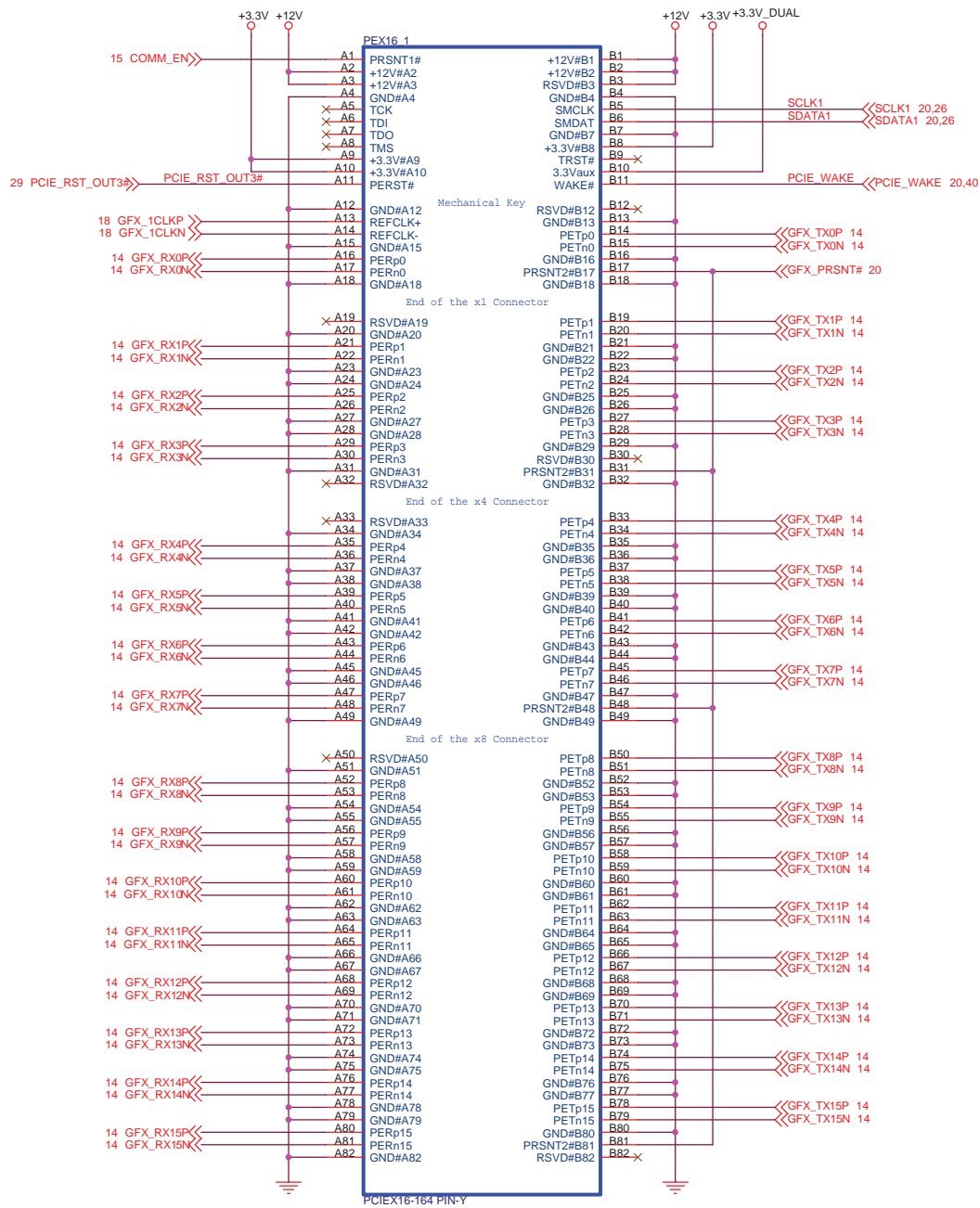


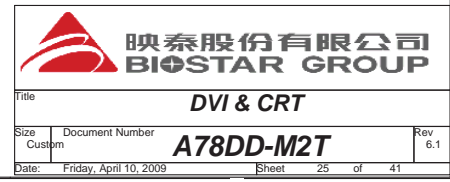


REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

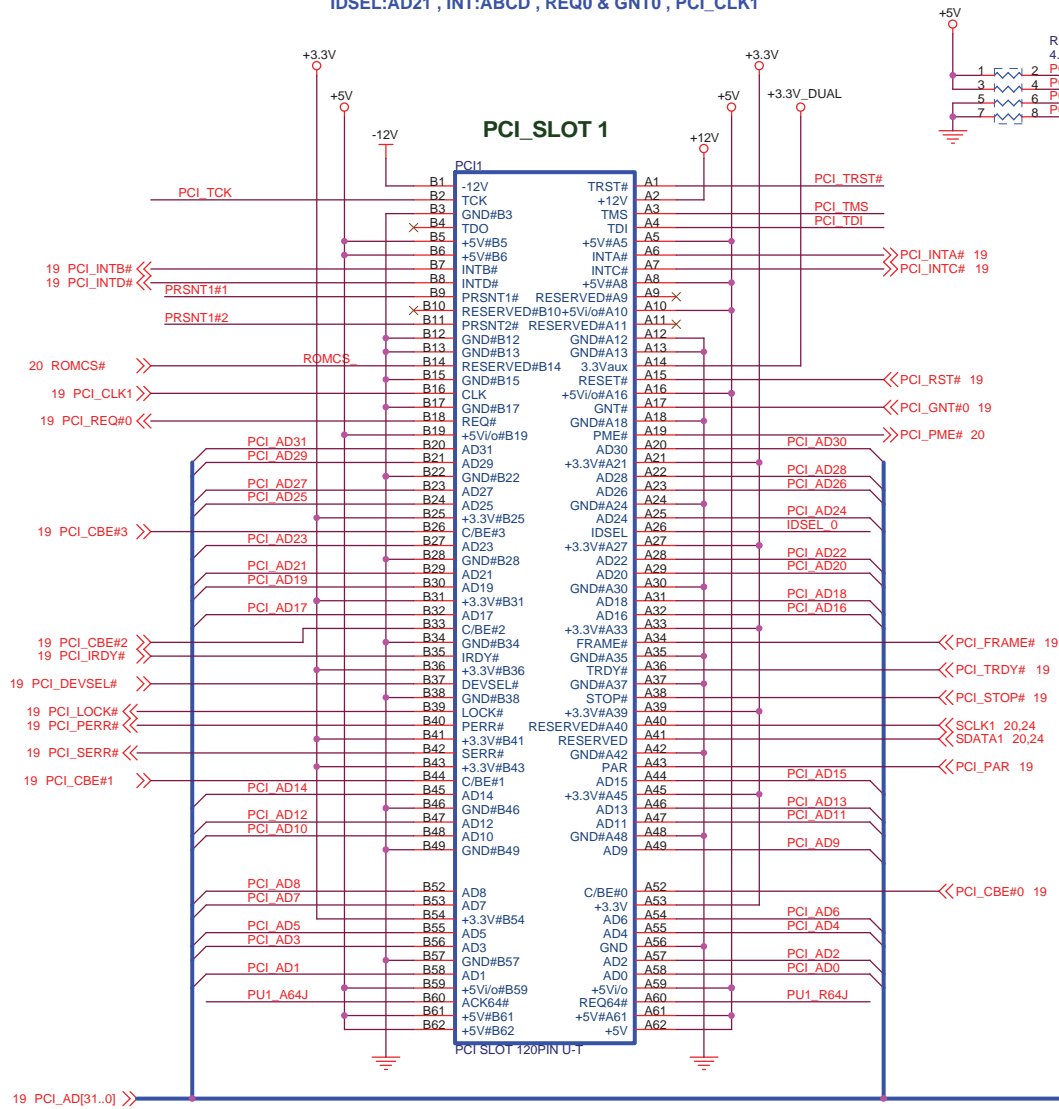
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED ADO Extreme	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, L = SPI ROM    DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	





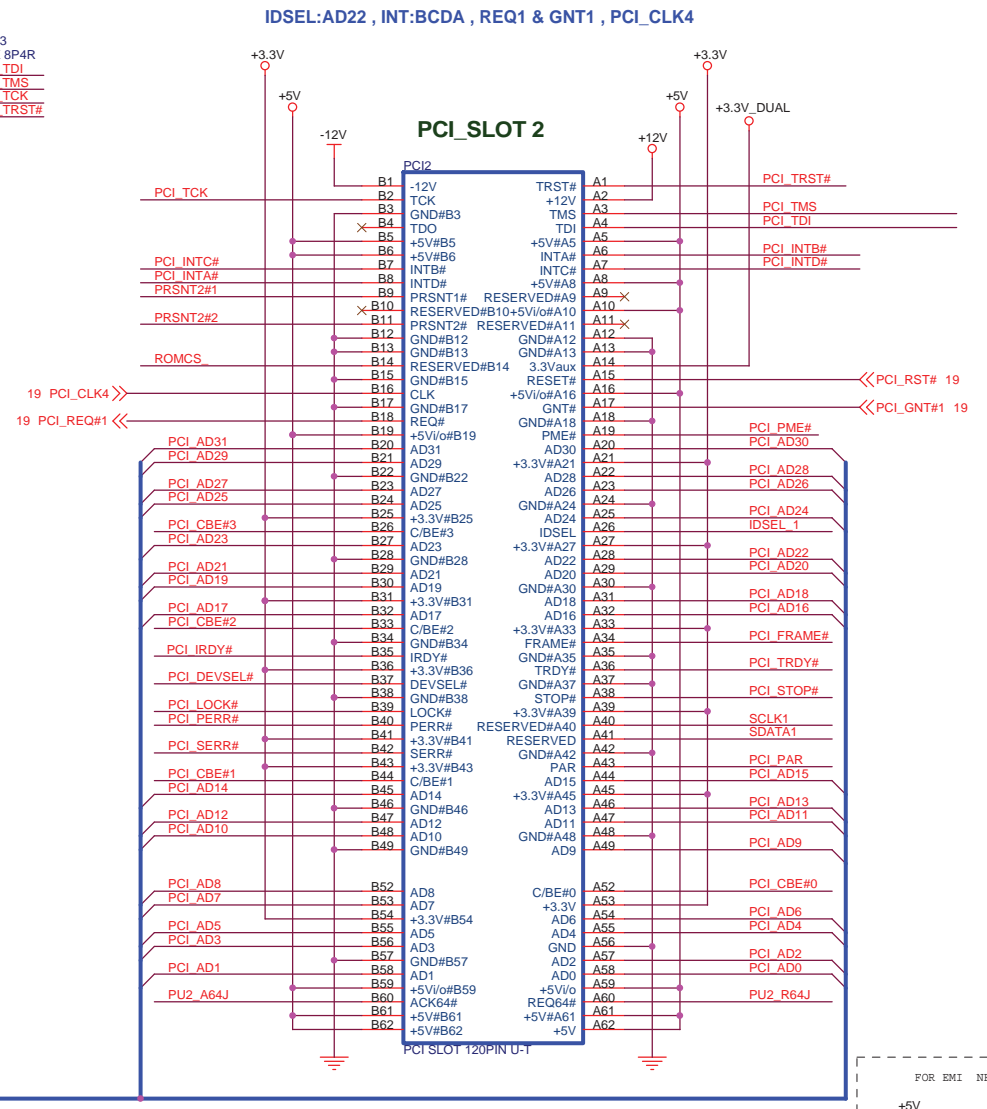
ISDEL:AD21, INT:ABCD, REQ0 & GNT0, PCI\_CLK1

### PCI\_SLOT 1

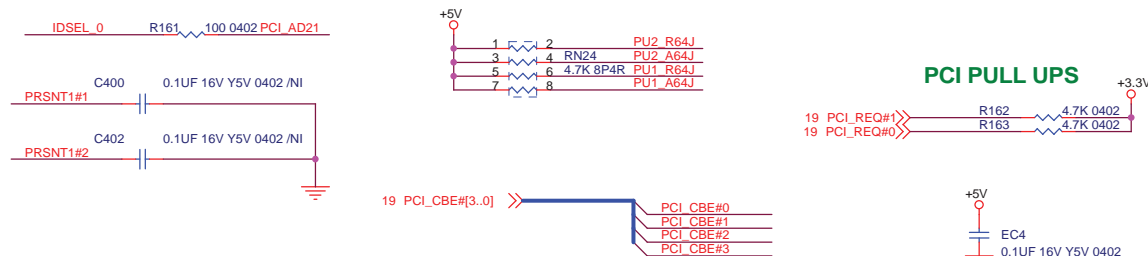


ISDEL:AD22, INT:BCDA, REQ1 & GNT1, PCI\_CLK4

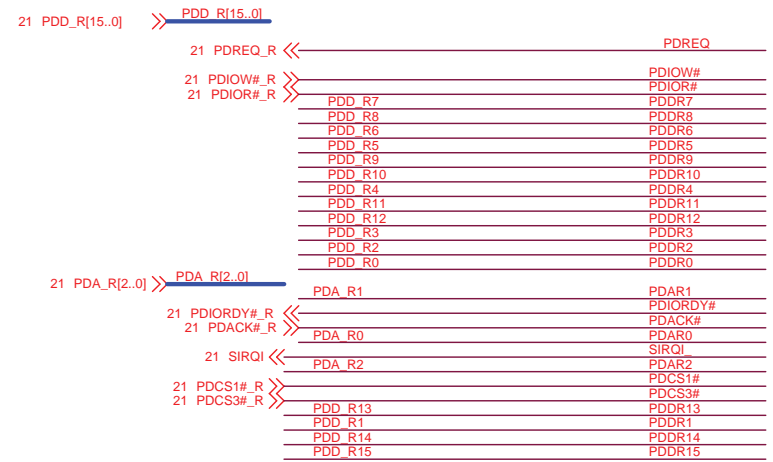
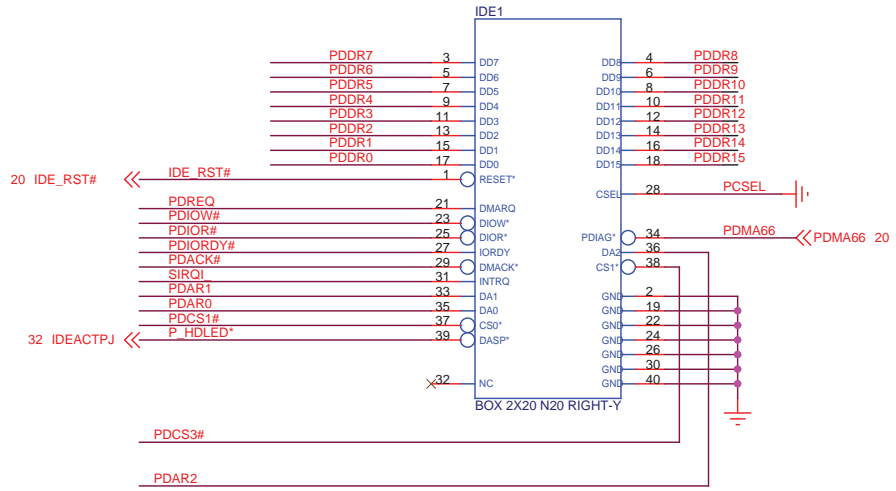
### PCI\_SLOT 2



### PCI PULL UPS




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1) MATCH WHOLE IDE LINES (BEFORE AND AFTER DAMPING RESISTORS) WITHIN 0.5"

2) ALL DAMPING RESISTORS CLOSE TO IDE CONNECTORS.



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Title

IDE ATA 133

Size B

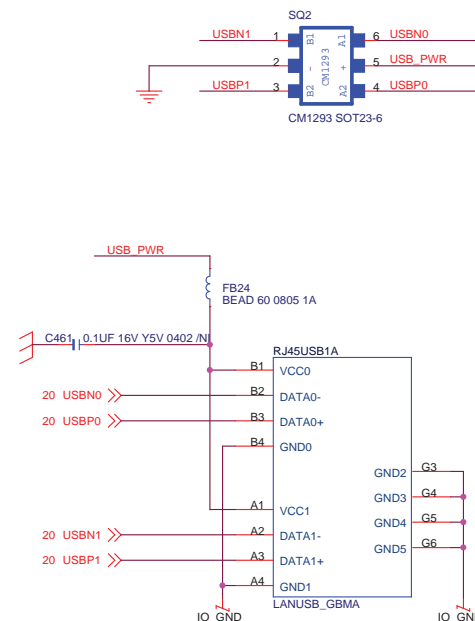
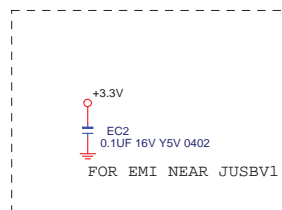
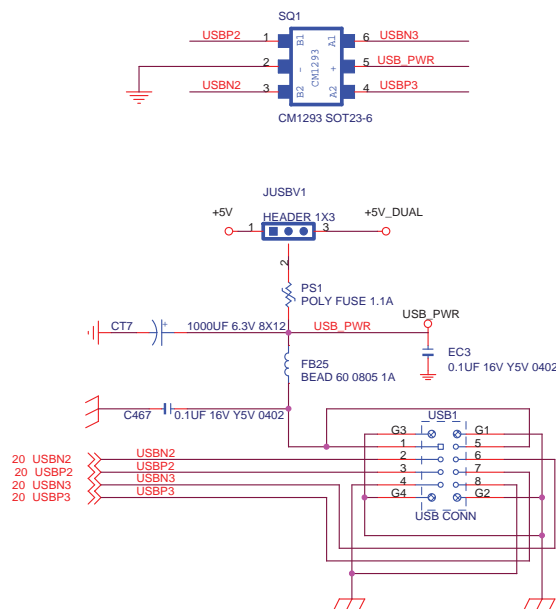
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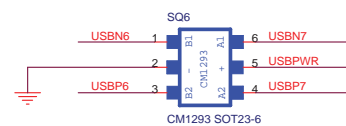
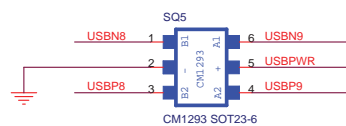
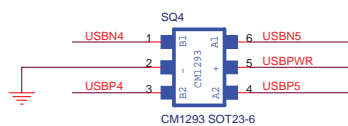
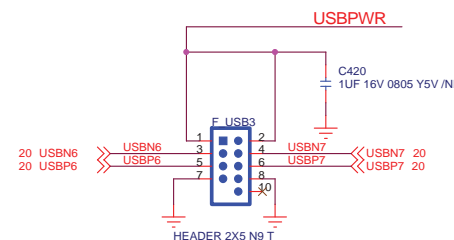
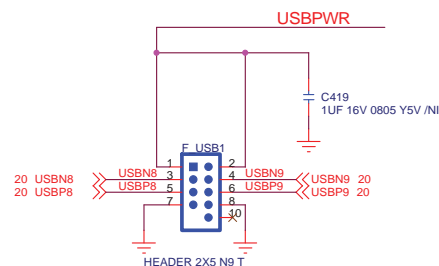
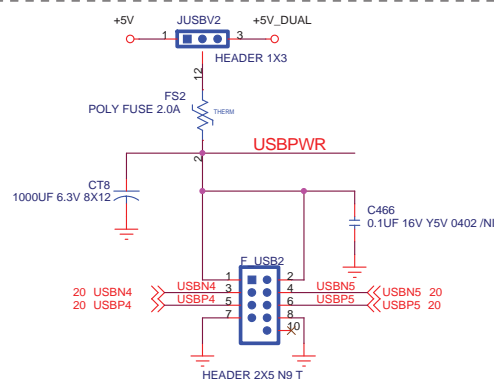
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BACK PANEL USB  
PLACE NEAR CONN

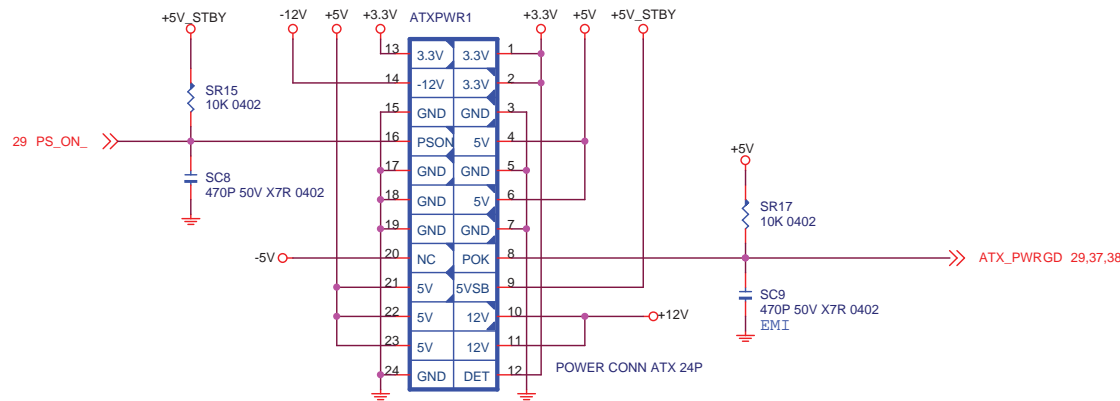


FRONT PANEL USB

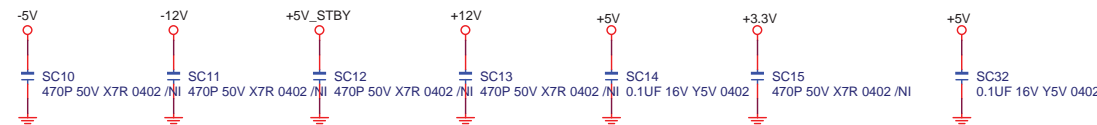




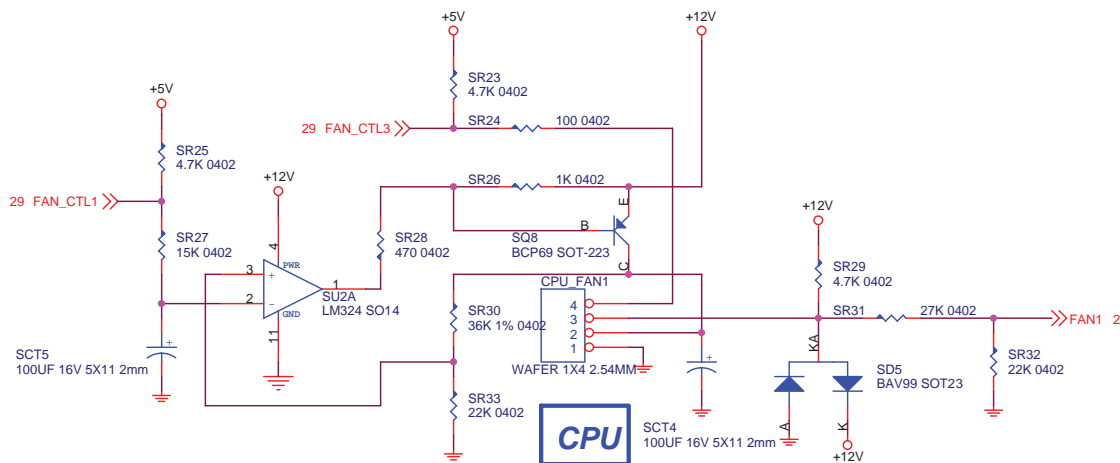
## POWER CONNECTOR



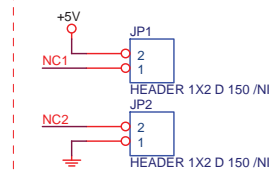
## POWER CONN DECOUPLING



## SYSTEM

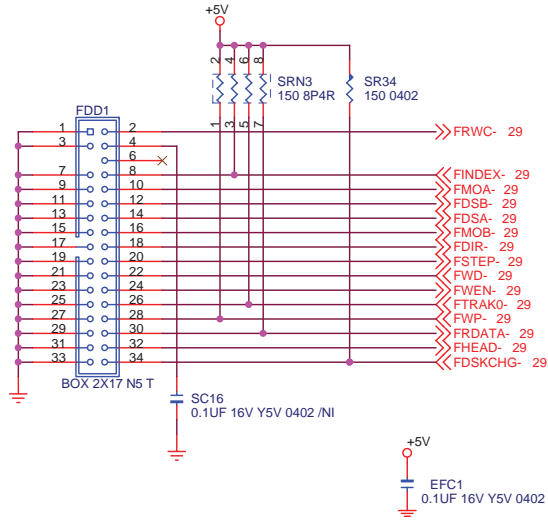


## Impedance Testing Coupon

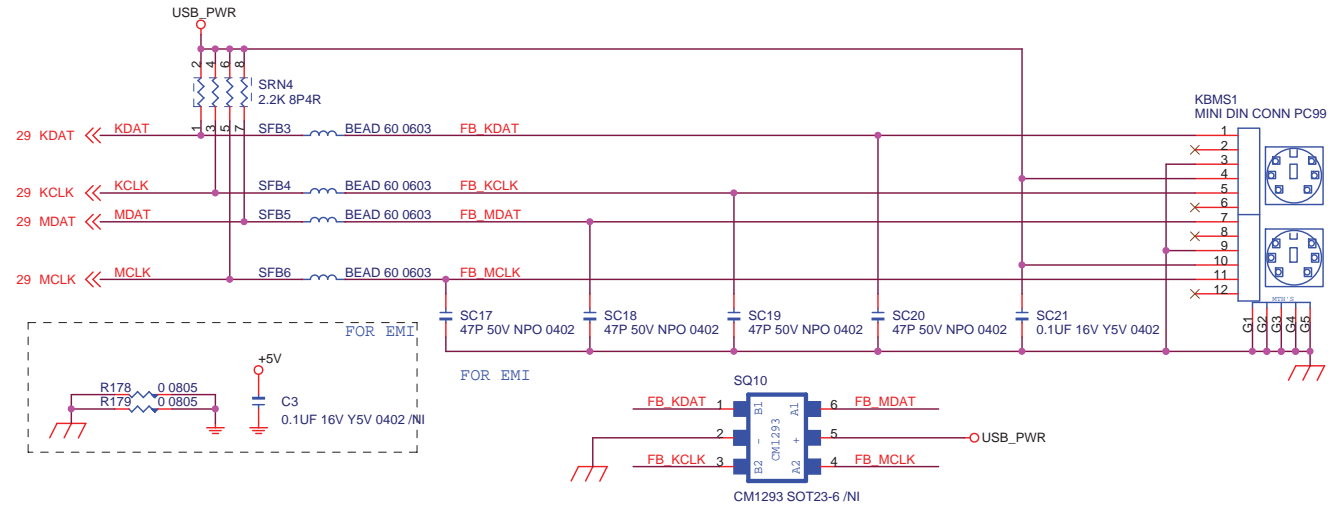


<b>FAN&amp;POWER CONN</b>		
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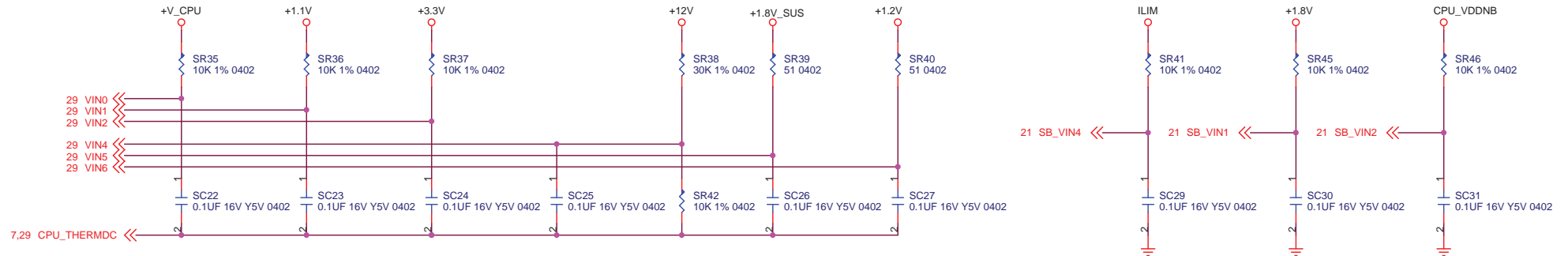
## FLOPPY CONNECTOR



## FOR KEYBOARD WITH MOUSE CONN.



## hardware monitor



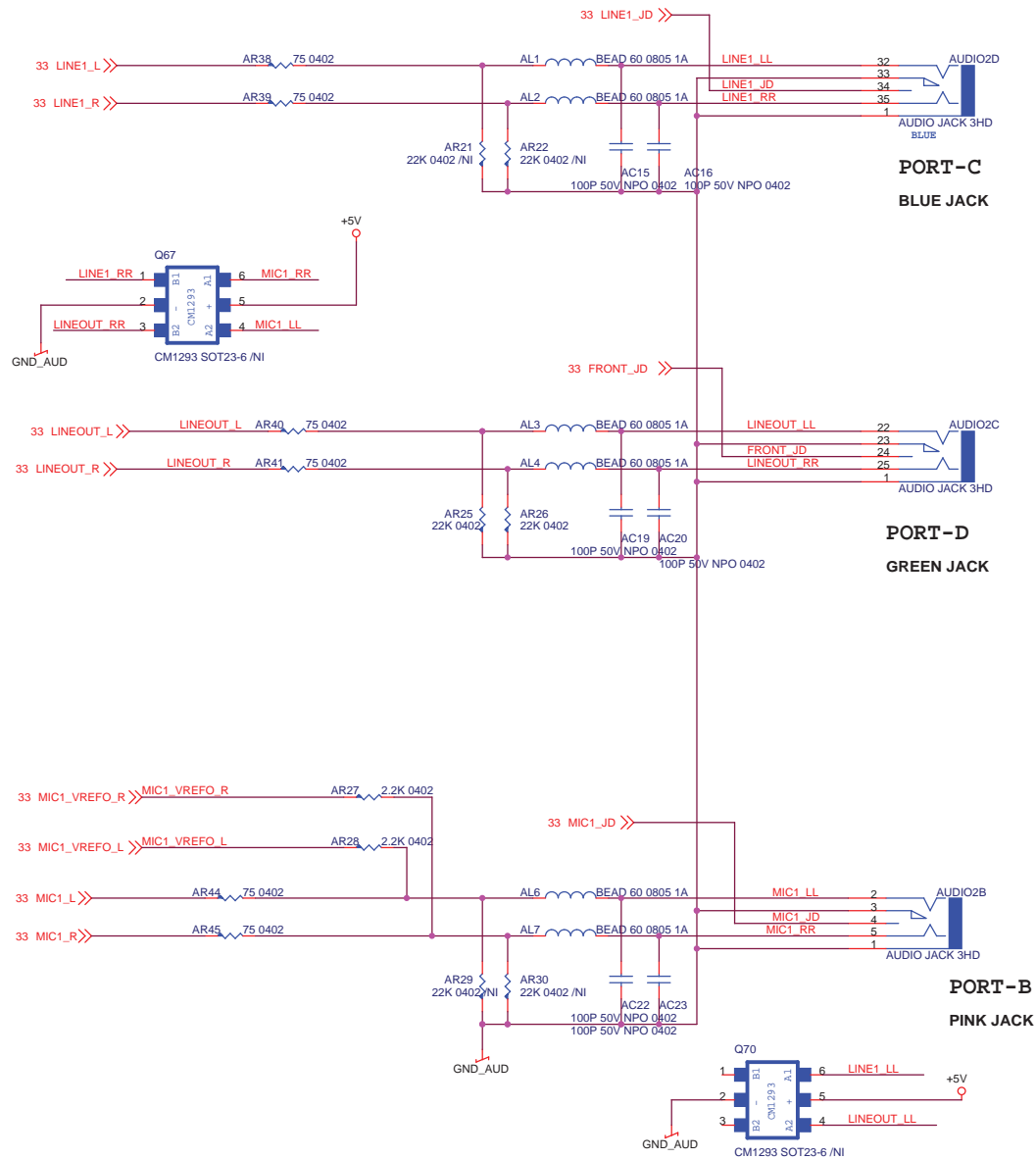
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FDD / PS2 CONN			
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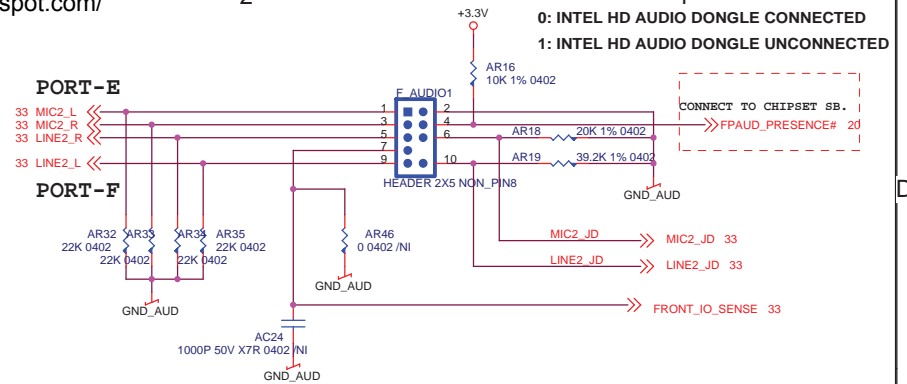


## Rear Panel Onboard Analog I/O

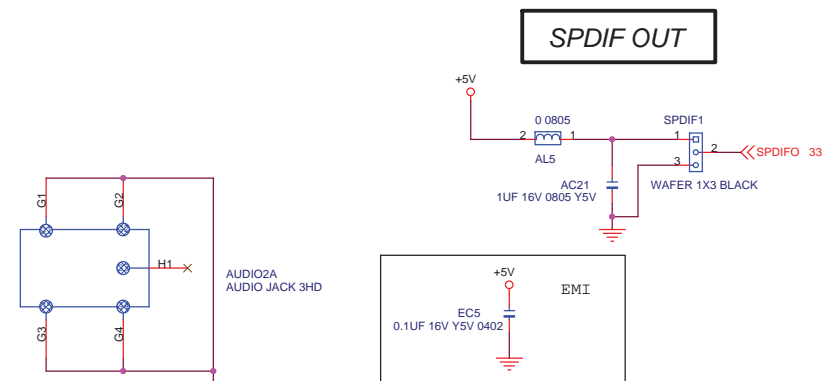
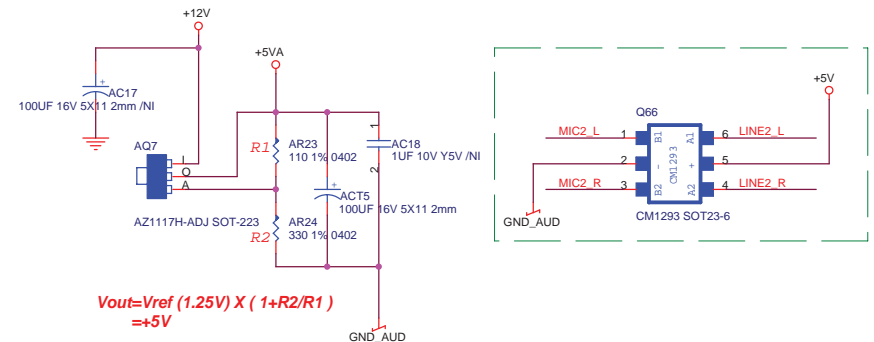
P07 : 3-Port & 6-Port Co-lay



\*ALC883/888: B, C, E, F ports support I/P & O/P function.  
But A, D, G, H ports not support MIC function.



## AUDIO ANALOG POWER



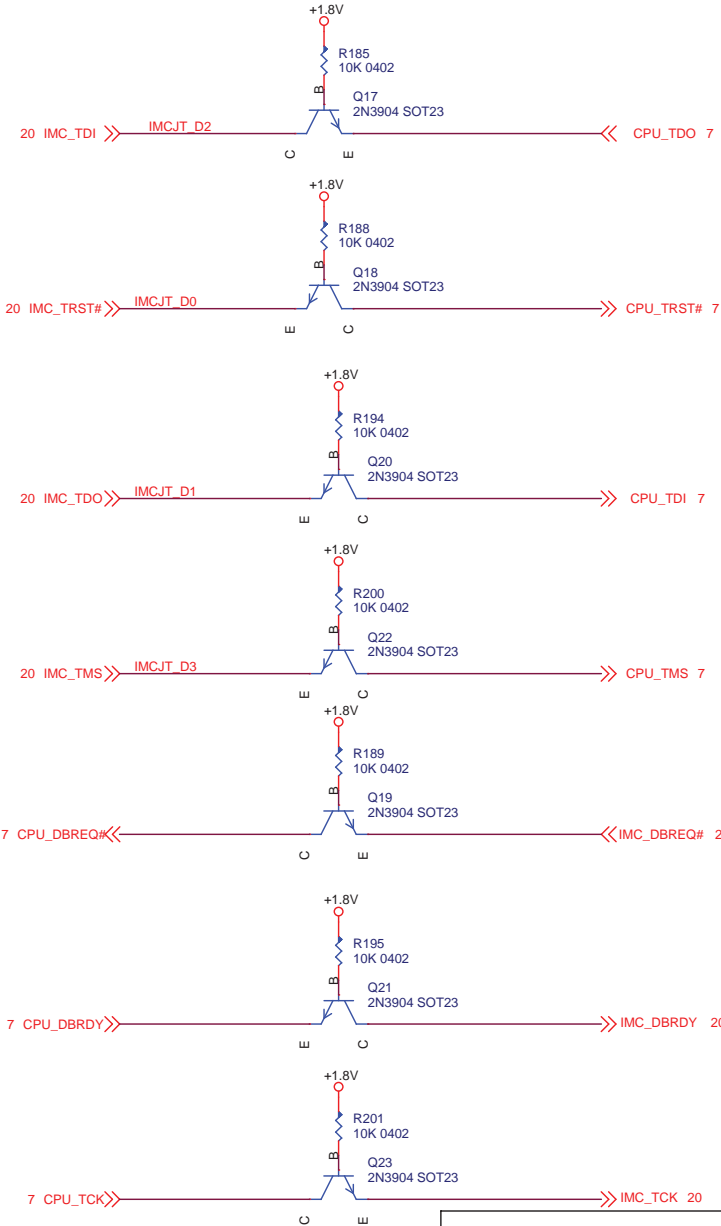
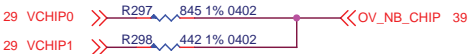
CPU_NB	VCPU_NB0	VCPU_NB1
Default	1	1
+0.1	0	1
+0.2	1	0
+0.3	0	0

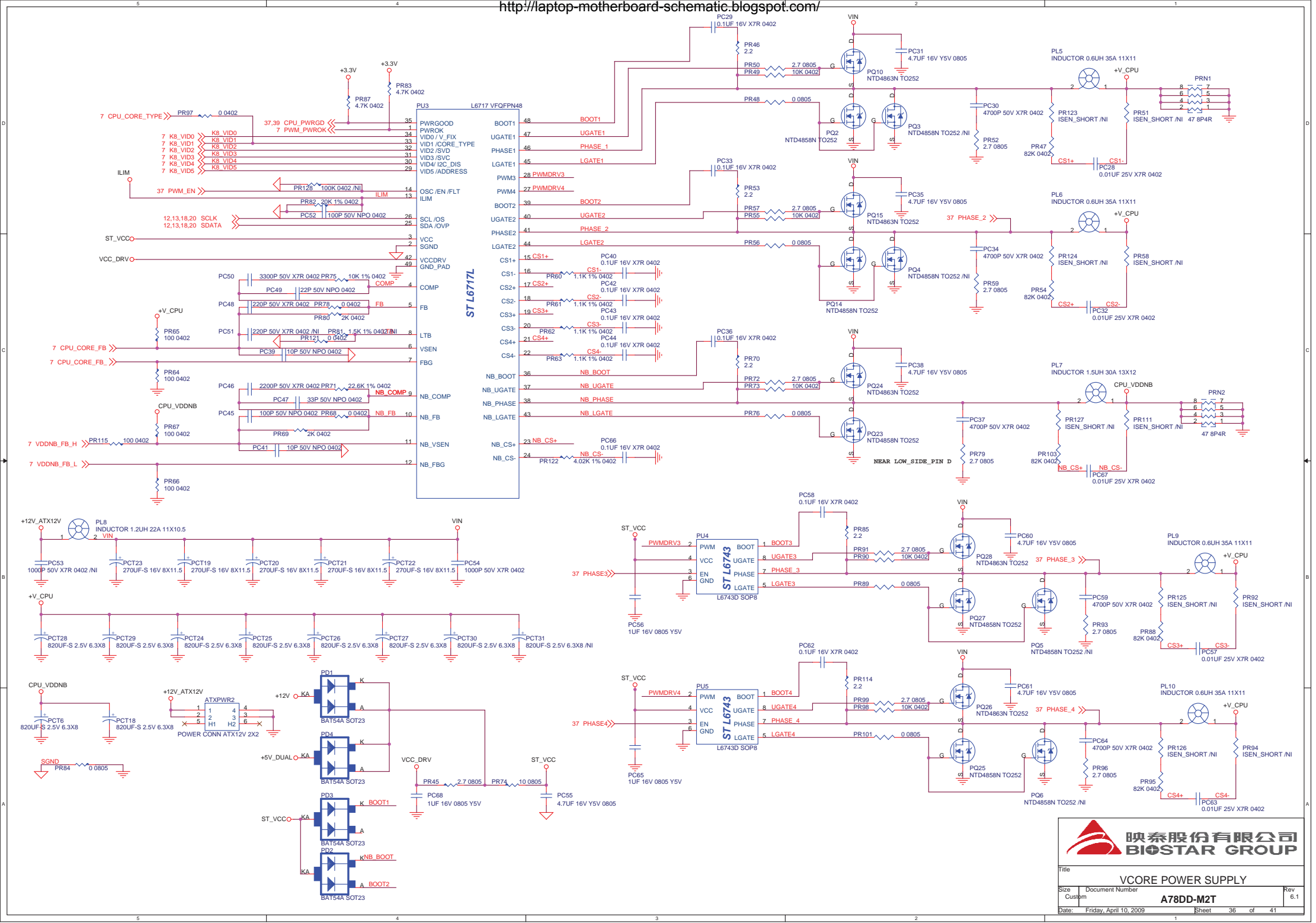
1.2V_HT	VHT0	VHT1
Default 1.23V	1	1
1.32V	0	1
1.43V	1	0
1.53V	0	0

SIDEPORT	VSP0	VSP1
Default 1.8V	1	1
1.9V	0	1
2.0V	1	0
2.1V	0	0

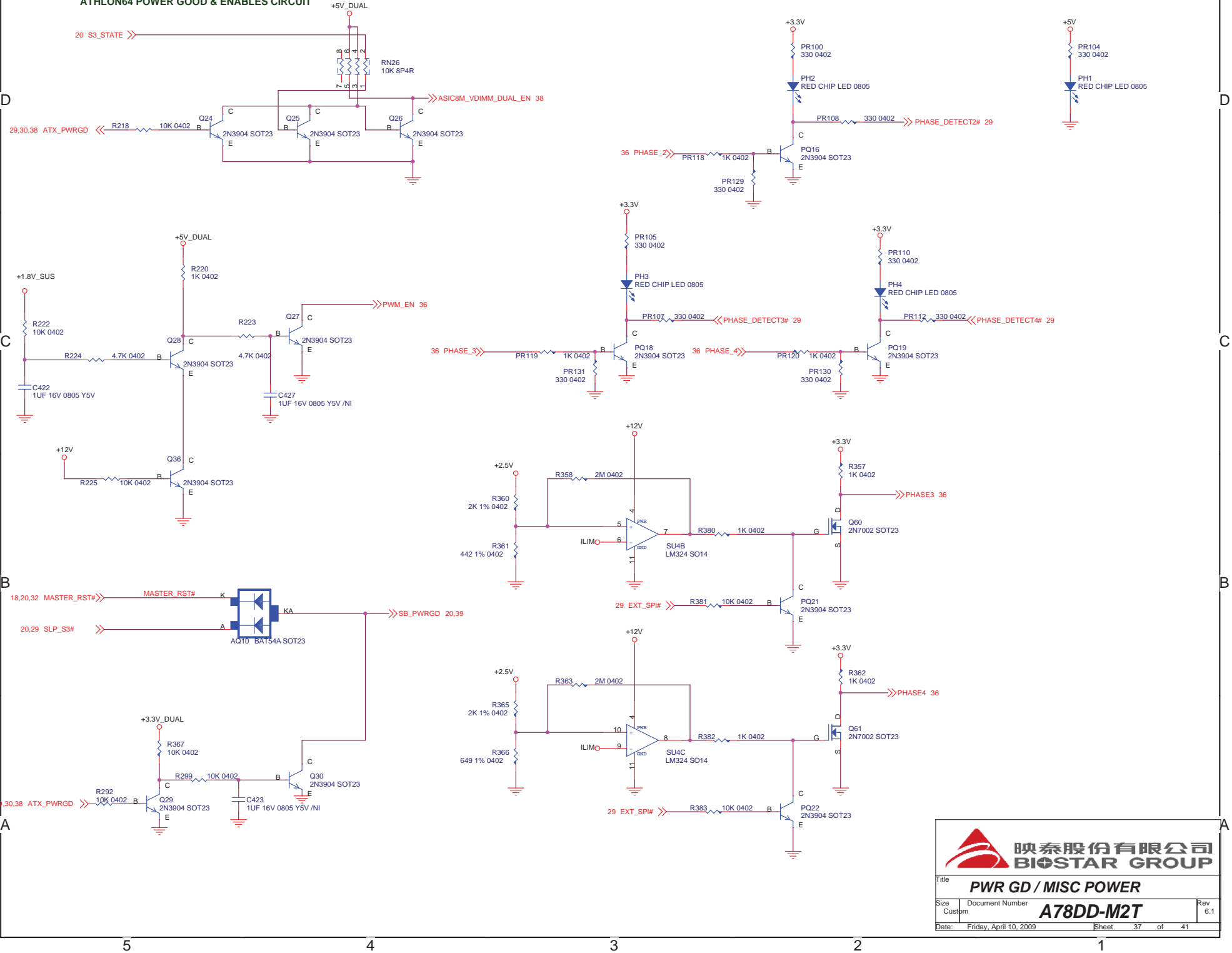
+1.8VDIMM_FB	VDIMM0	VDIMM1	VDIMM2
Default 1.95V	1	1	1
2.05V	0	1	1
2.15V	1	0	1
2.25V	0	0	1
2.35V	1	1	0
2.45V	0	1	0
2.55V	1	0	0
2.65V	0	0	0

NB CORE	OV_CHIP1	OV_CHIP0
+1.25V	1	1
+1.35V	0	1
+1.45V	1	0
+1.55V	0	0



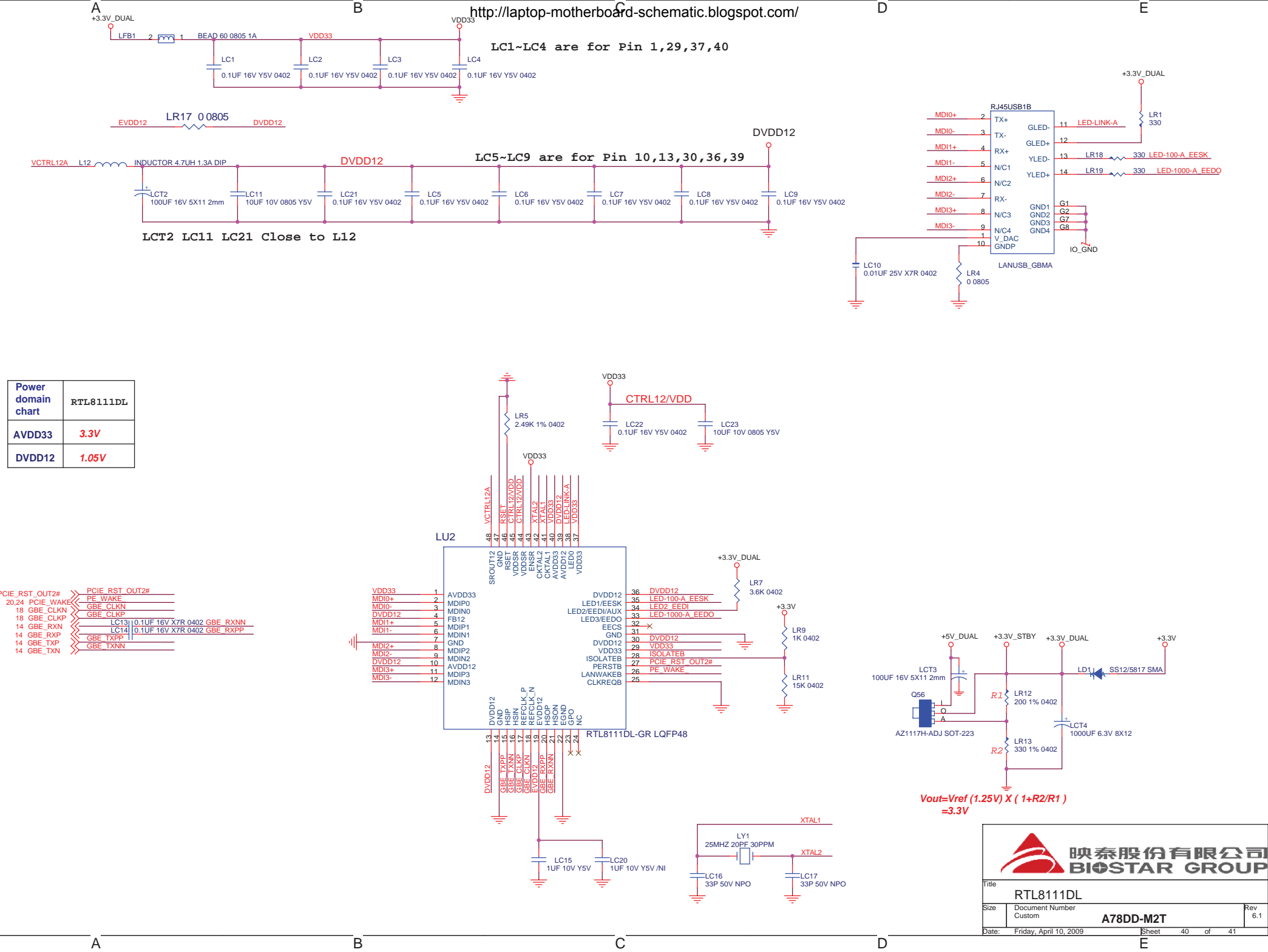


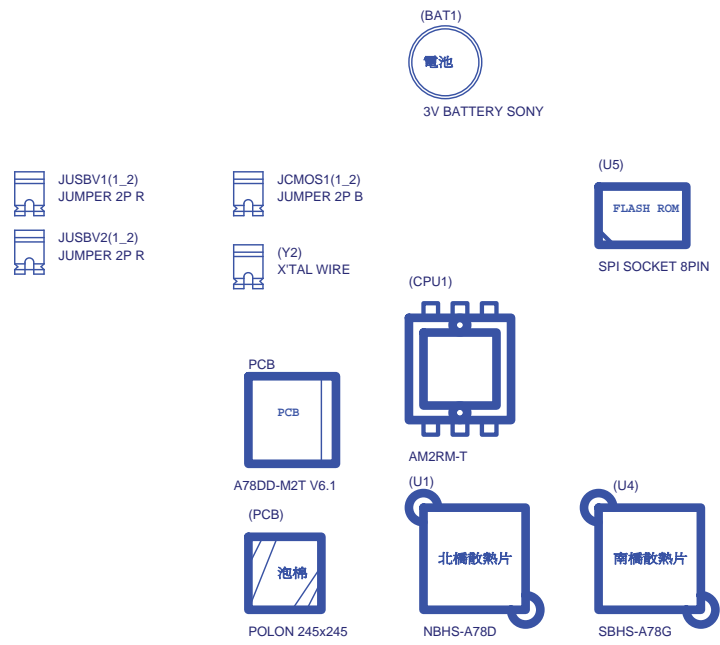
# ATHLON64 POWER GOOD & ENABES CIRCUIT











New JPANEL1  
JPANEL1 2\*8  
JPANEL1(9\_10) JPANEL1(15\_16)  
HEADER 1X2 HEADER 1X2  
JPANEL1(11\_14)  
PLED  
JPANEL1(1\_4) JPANEL1(5\_6)JPANEL1(7\_8)  
SPK HLED RST